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Test Equipment Repair & Calibration

## **HP 8560E**

HP 8560E Service Manual large scan Part2of2

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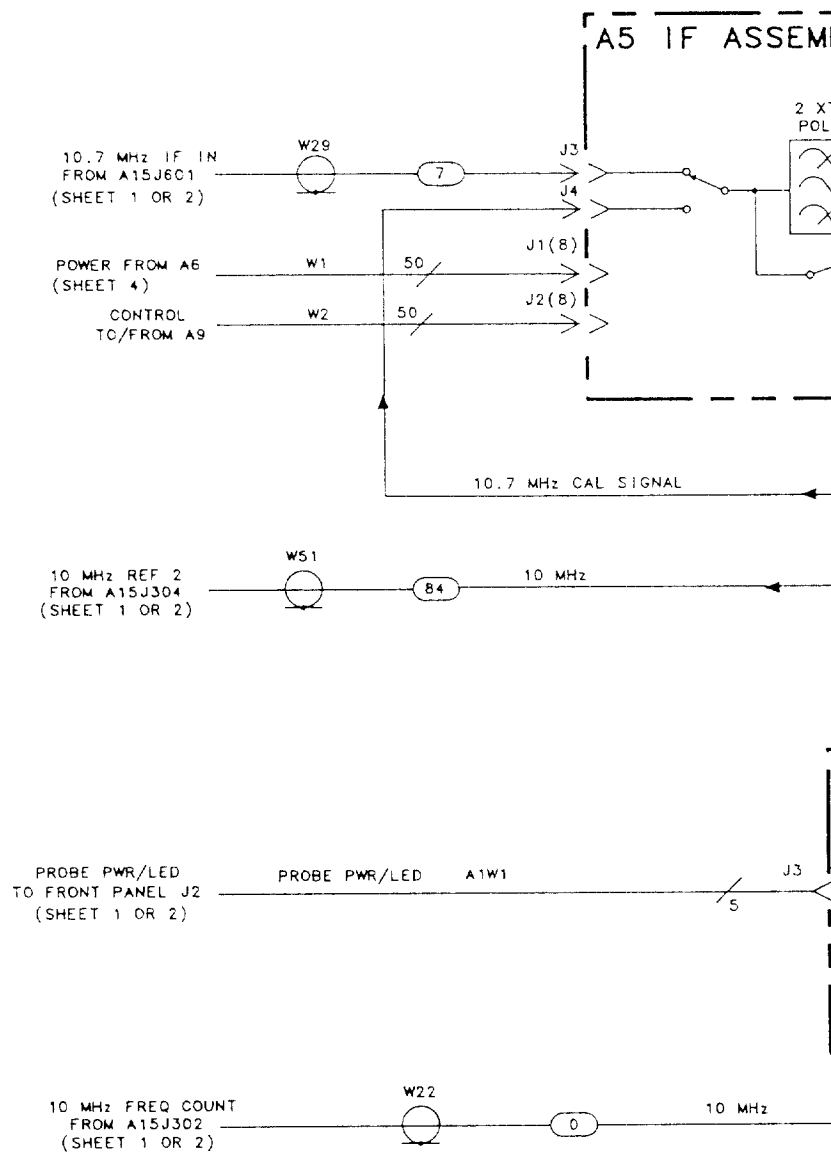
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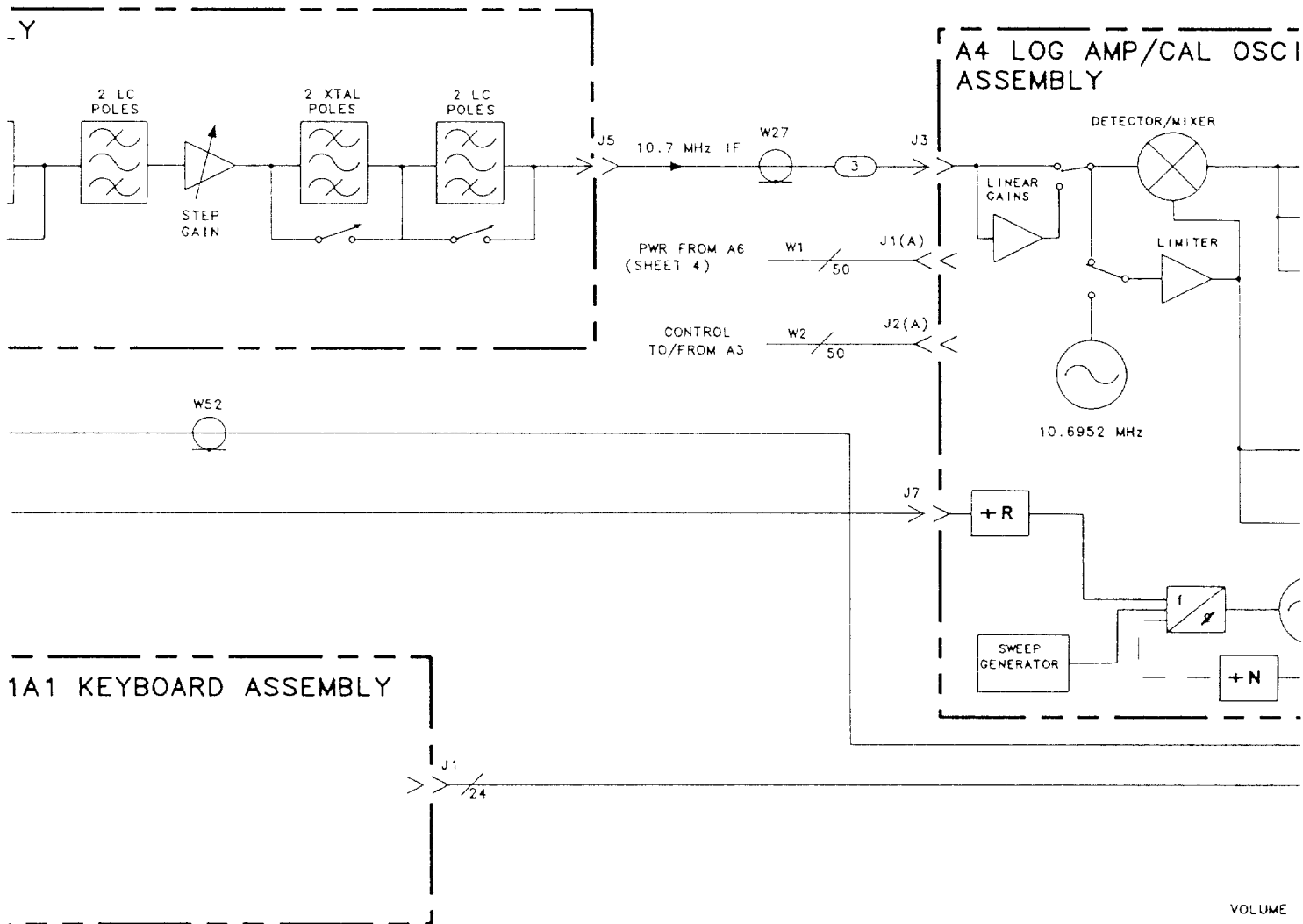
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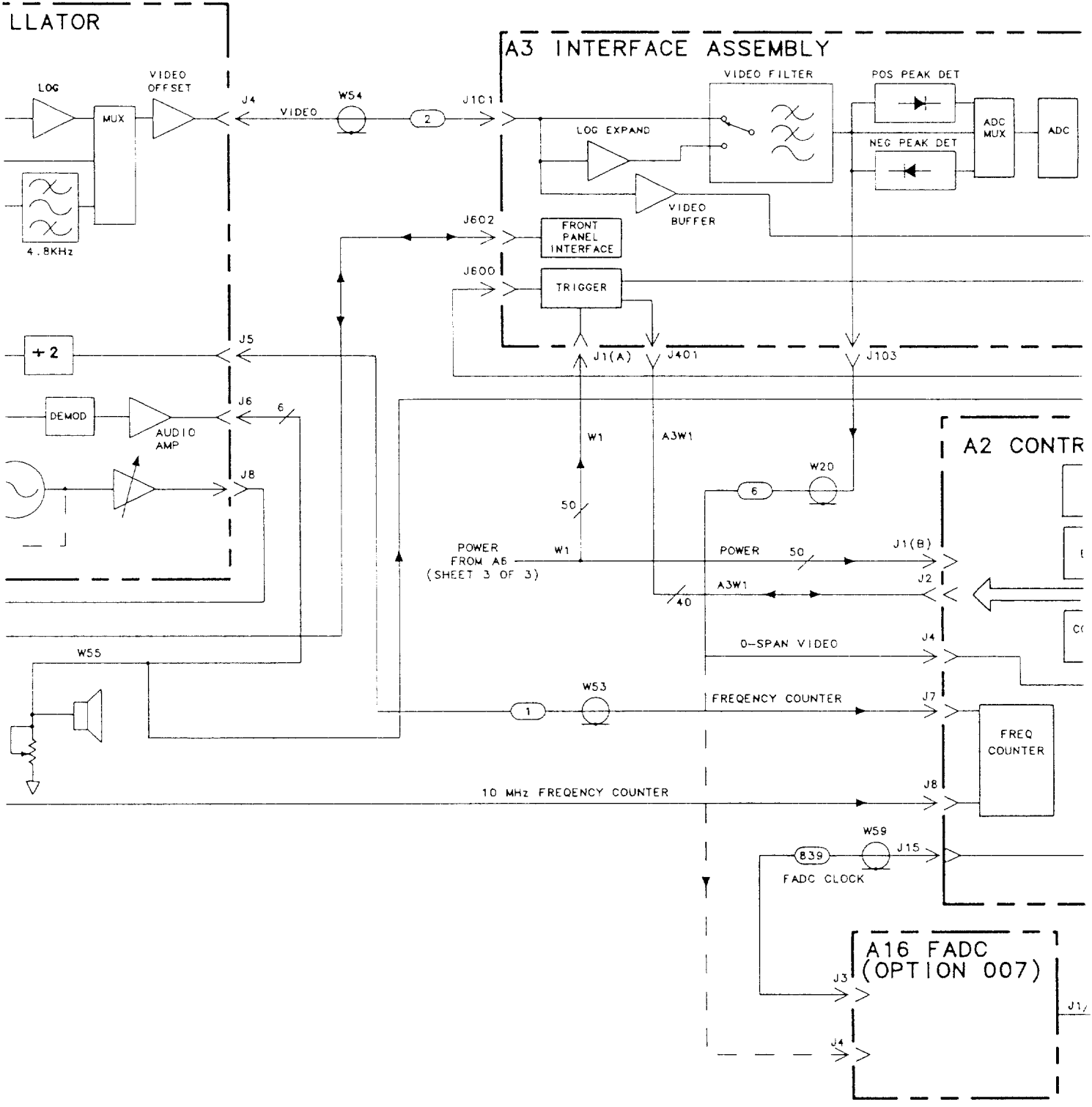
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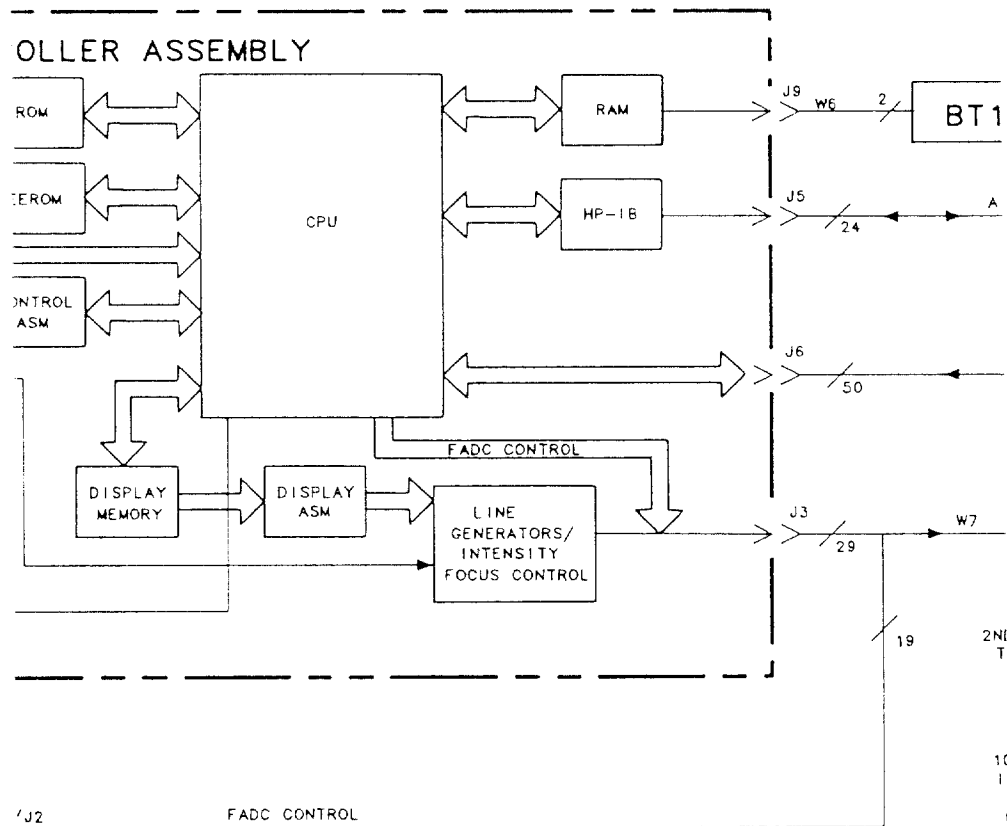
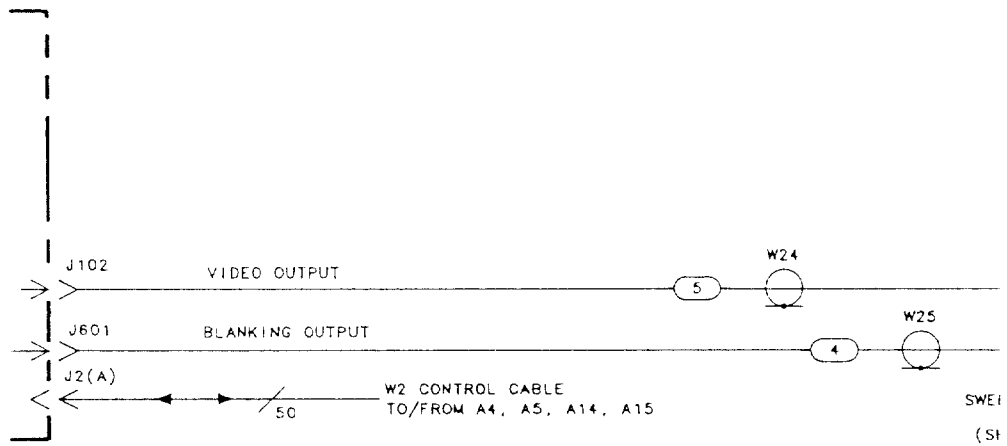
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# 8560E OVERALL BLOCK DIAGRAM (SHEET 3 OF 4)









FIGU

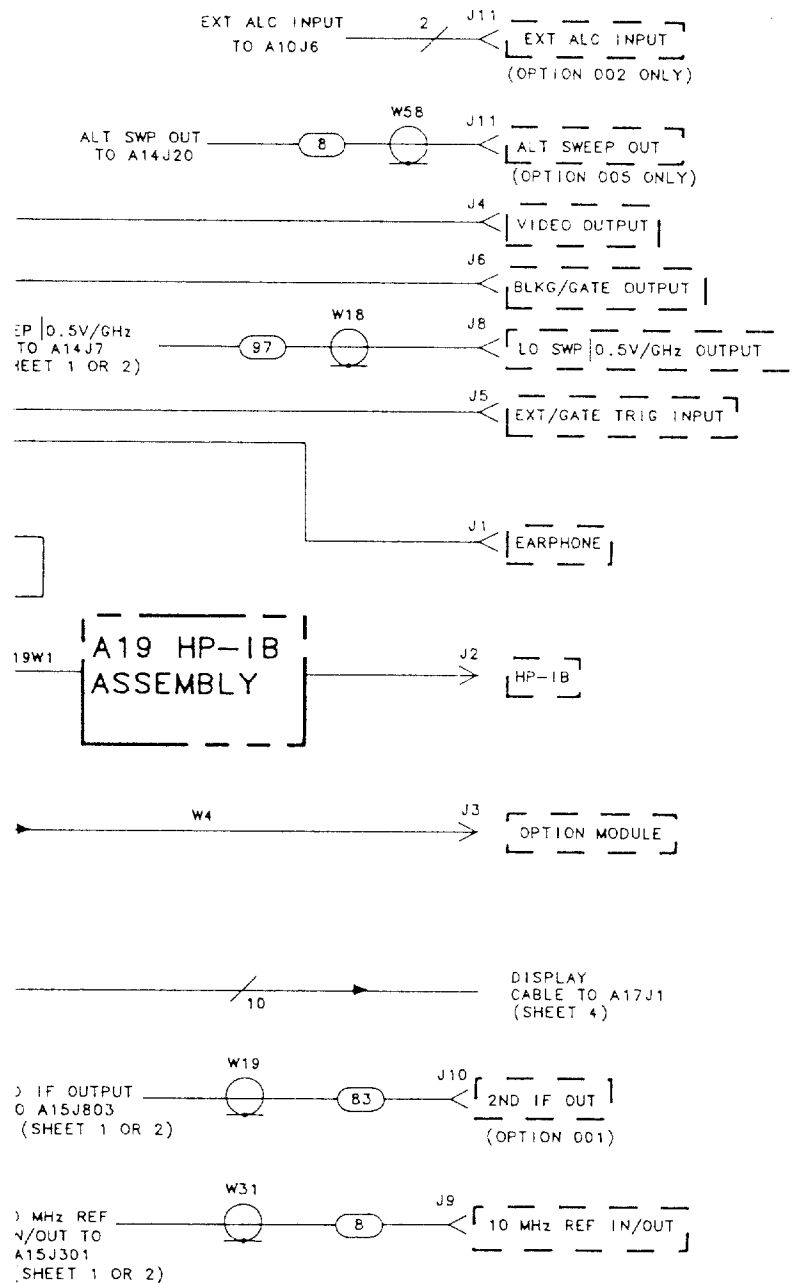
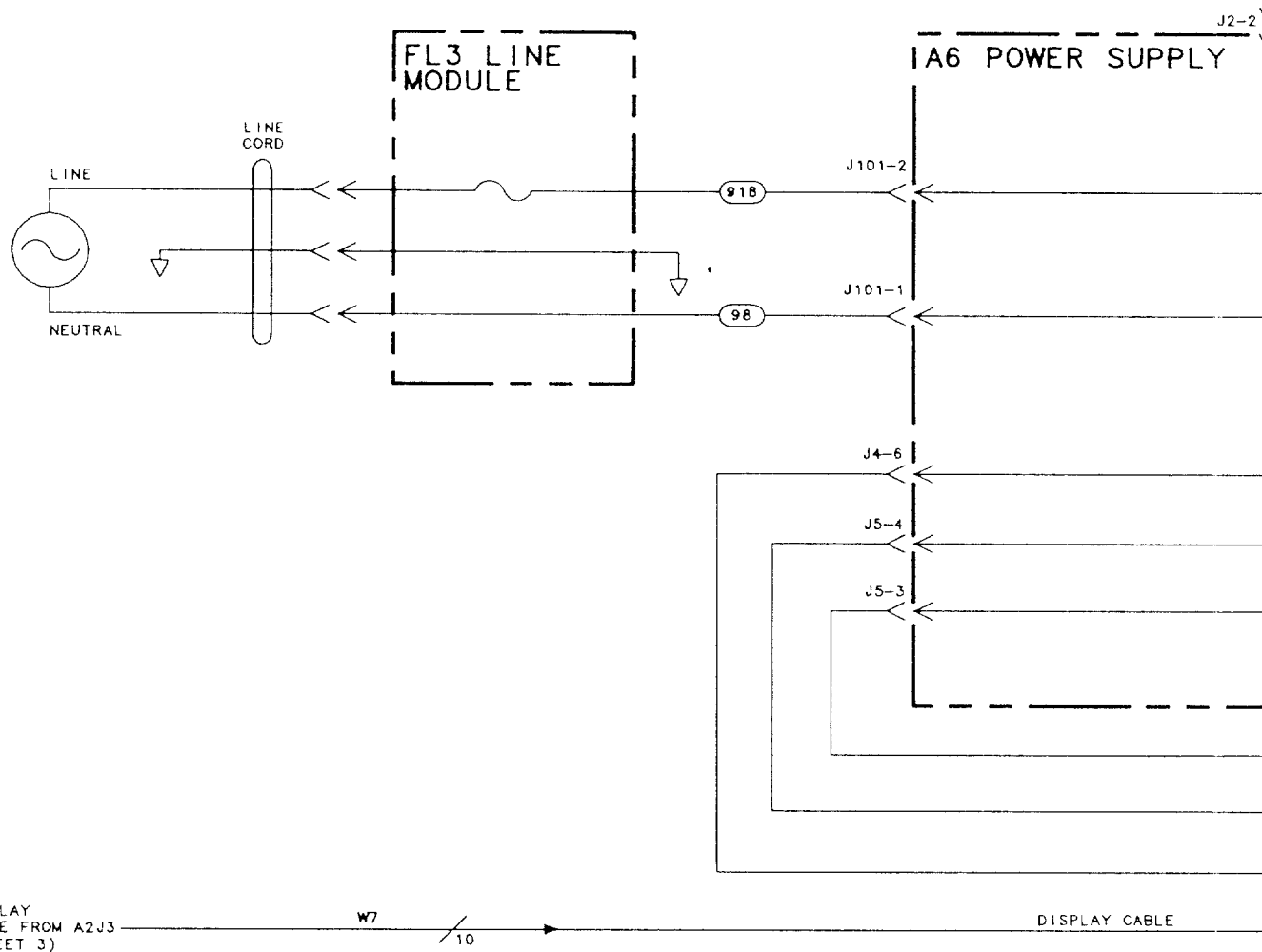
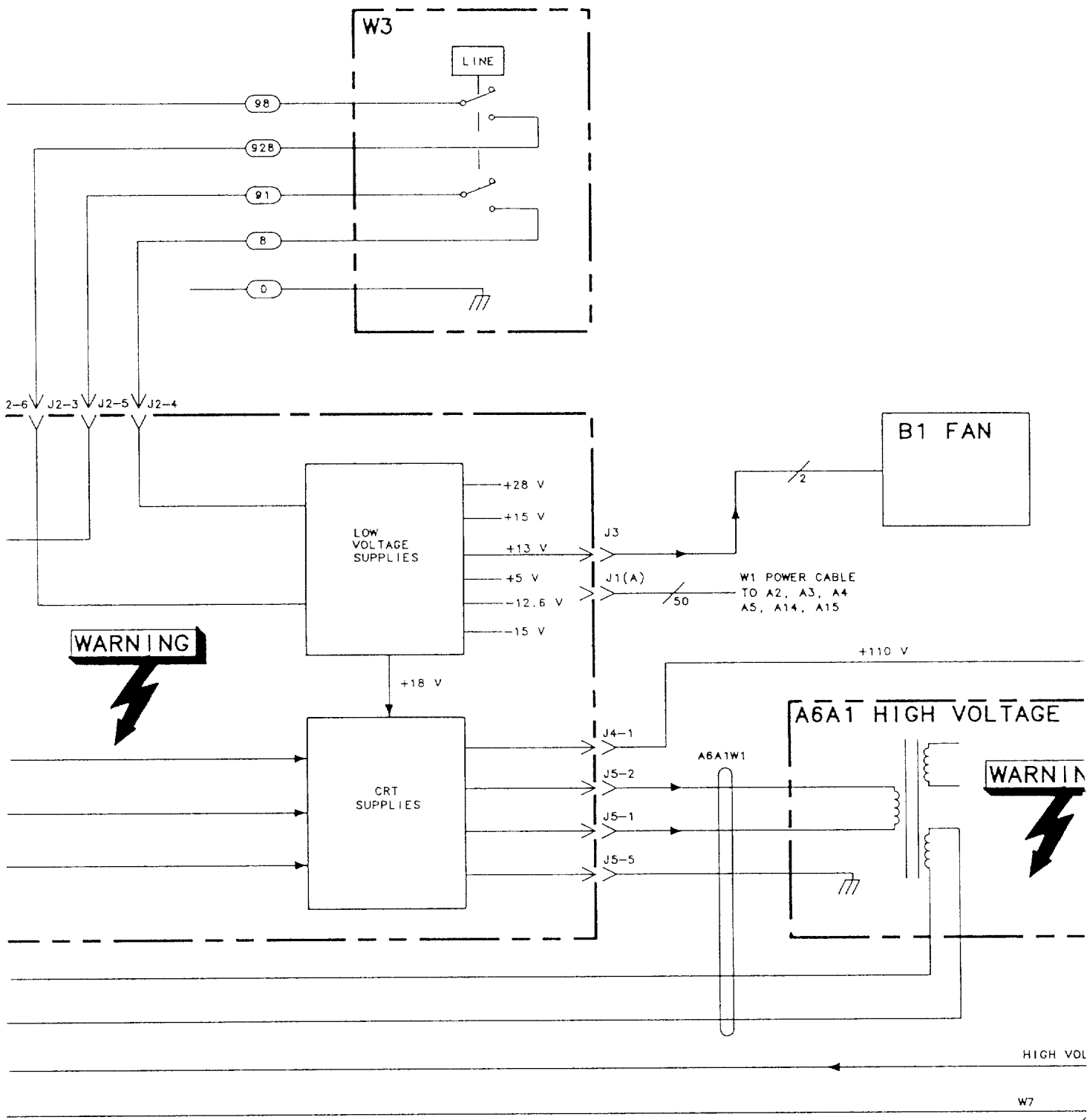
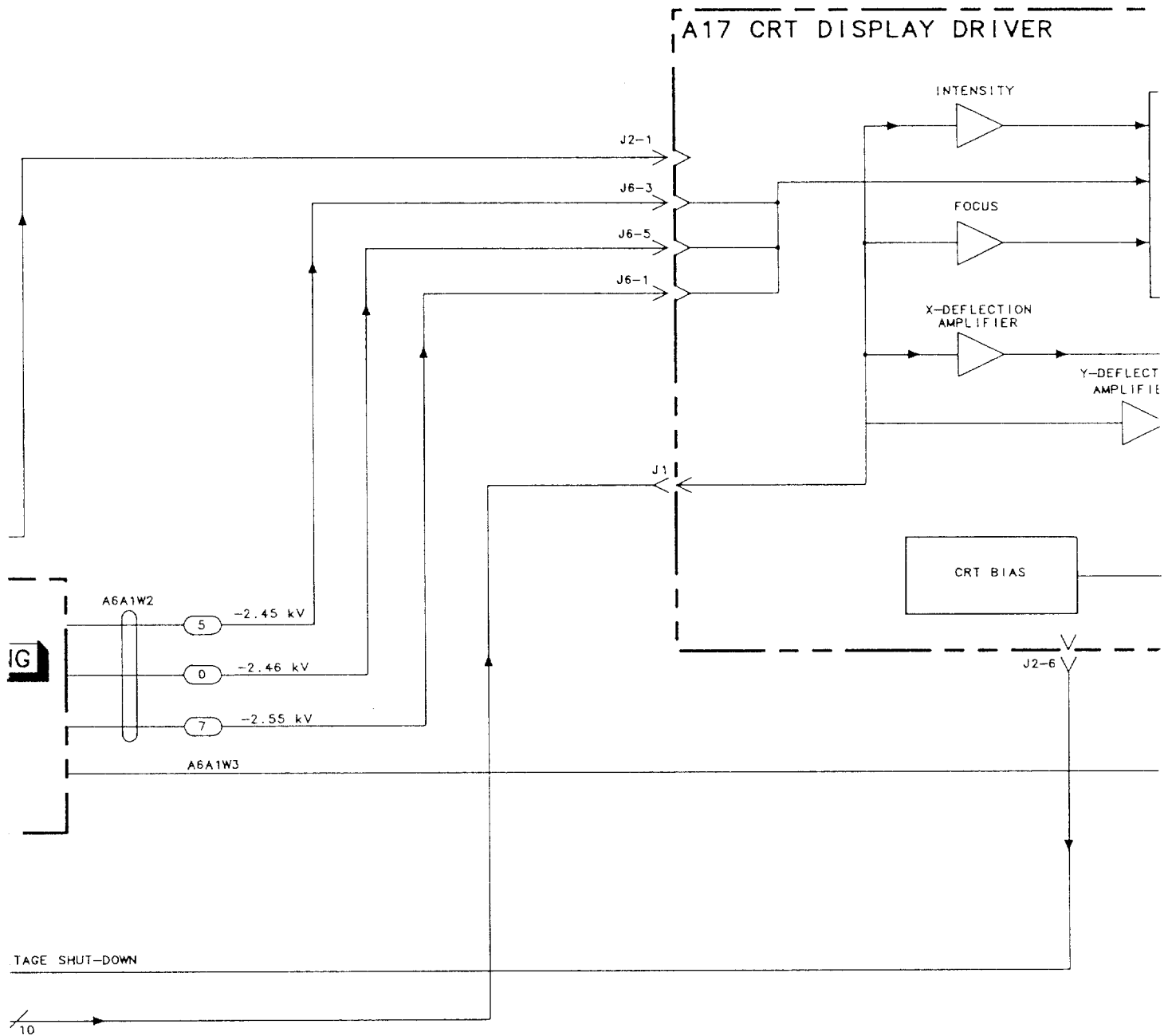


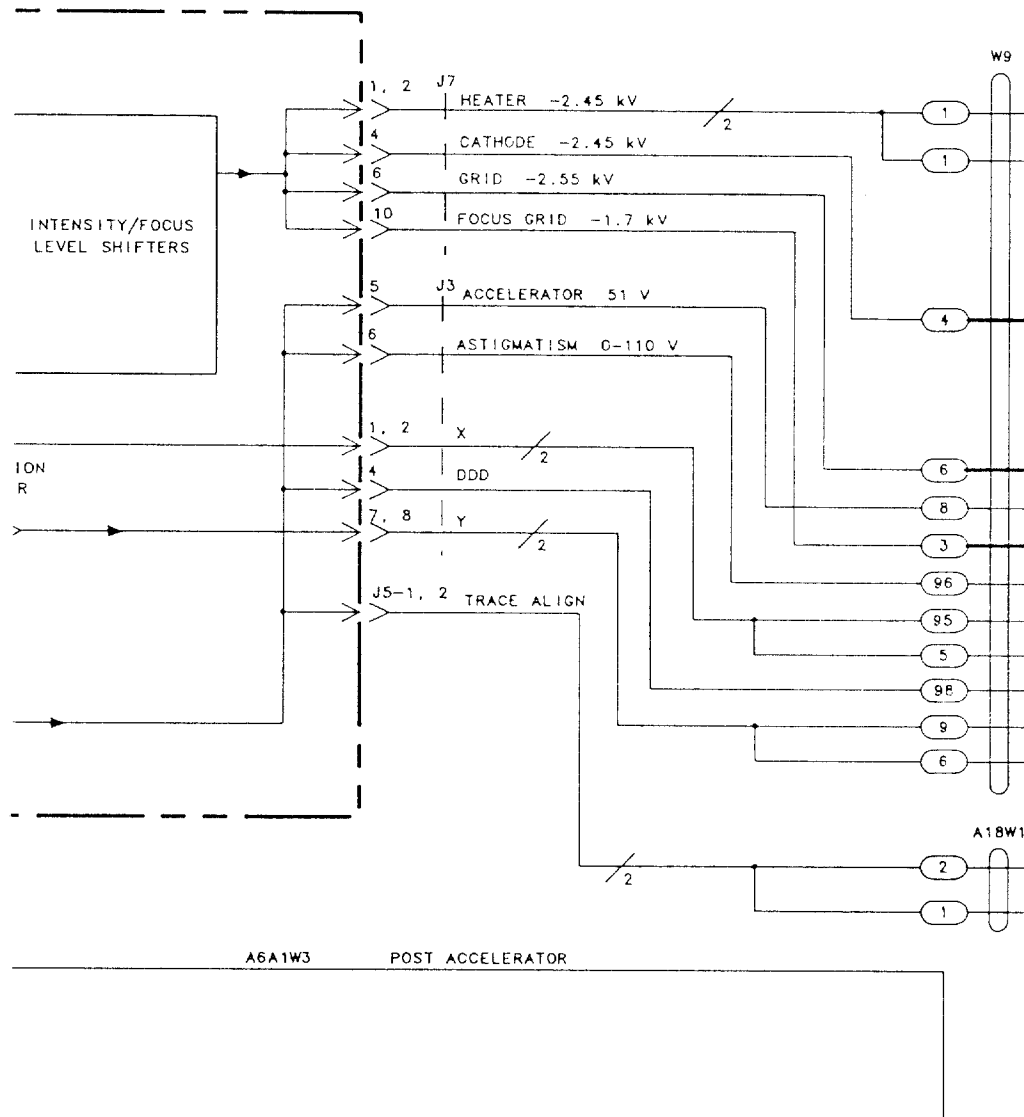
FIGURE 6-7. HP 8560E OVERALL BLOCK DIAGRAM (SHEET 3 OF 4)

8560E OVERALL BLOCK DIAGRAM  
(SHEET 4 OF 4)



# A17 CRT DISPLAY DRIVER





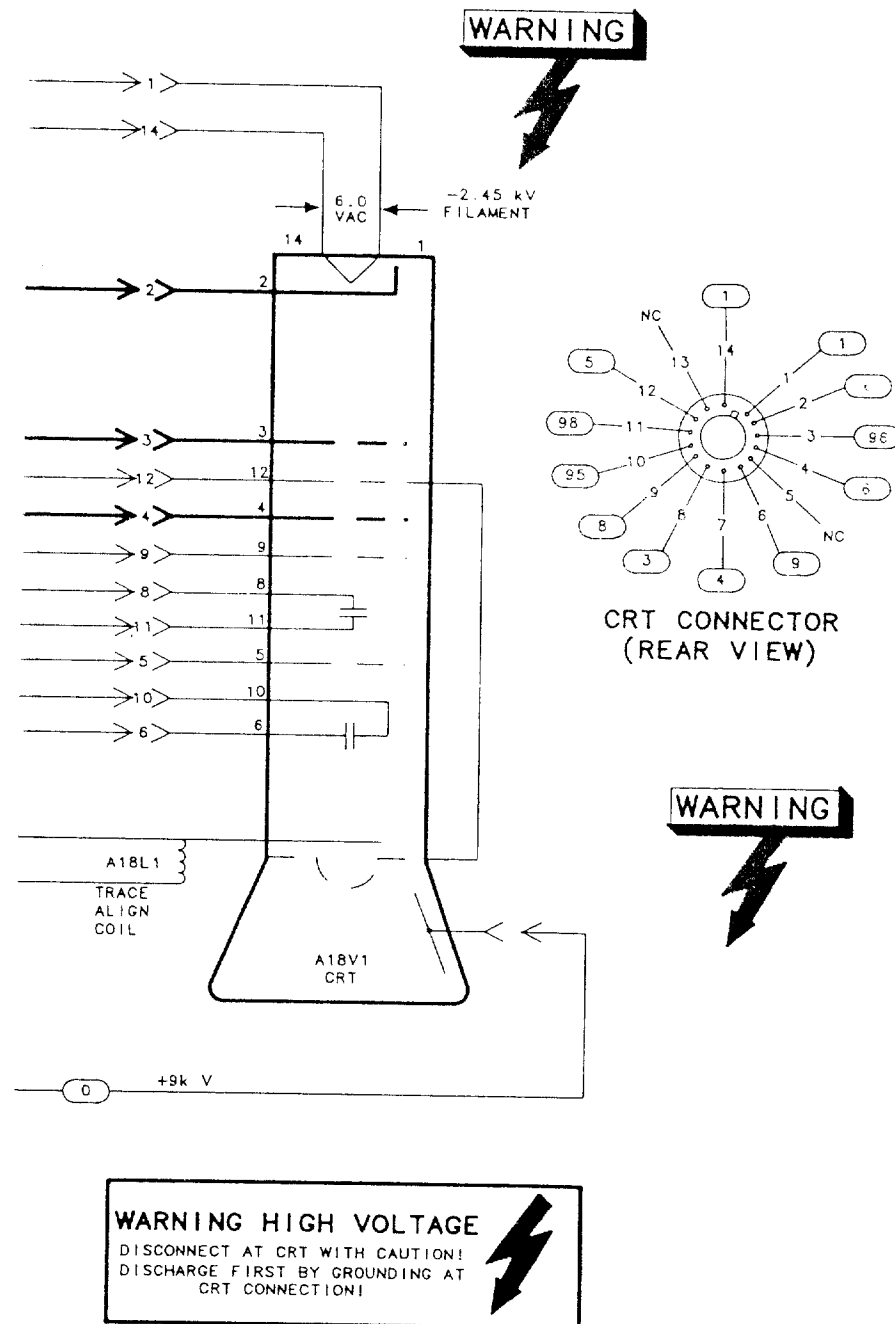


FIGURE 6-7. HP 8560E OVERALL BLOCK DIAGRAM (SHEET 4 OF 4)

## ADC/Interface Section

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The ADC/Interface section includes the A1A1 keyboard, A1A2 RPG (rotary pulse generator), A3 interface, and A16 fast ADC (Option 007) assemblies. Table 7-1 lists signal versus pin numbers for control cable W2.

- Troubleshooting Using the TAM
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- A16 Assembly's Fast ADC Control Circuits (Option 007)
  - CPU Interface and Control Registers
  - Reference Clock
  - Clock and Sample Rate Generator

Trigger  
 16-Bit Post-Trigger Counter  
 15-Bit (32 K) Circular Address Counter  
 Video Trigger Comparator

**Table 7-1. W2 Control Cable Connections**

| Signal       | A3J2 (pins) | A4J2 (pins) | A5J2 (pins) | A14J2 (pins) | A15J2 (pins) |
|--------------|-------------|-------------|-------------|--------------|--------------|
| D0           | 1*          | 1           | 50          | 1            | 1            |
| D GND        | 2*          | 2           | 49          | 2            | 2            |
| D1           | 3*          | 3           | 48          | 3            | 3            |
| D2           | 4*          | 4           | 47          | 4            | 4            |
| D3           | 5*          | 5           | 46          | 5            | 5            |
| D4           | 6*          | 6           | 45          | 6            | 6            |
| D GND        | 7*          | 7           | 44          | 7            | 7            |
| D5           | 8*          | 8           | 43          | 8            | 8            |
| D6           | 9*          | 9           | 42          | 9            | 9            |
| D7           | 10*         | 10          | 41          | 10           | 10           |
| A0           | 11*         | 11          | 40          | 11           | 11           |
| D GND        | 12*         | 12          | 39          | 12           | 12           |
| A1           | 13*         | —           | 38          | 13           | 13           |
| A2           | 14*         | —           | 37          | 14           | 14           |
| A3           | 15*         | 15          | 36          | 15           | 15           |
| A4           | 16*         | —           | 35          | 16           | 16           |
| D GND        | 17*         | 17          | 34          | 17           | 17           |
| A5           | 18*         | —           | 33          | 18           | —            |
| A6           | 19*         | —           | 32          | —            | —            |
| A7           | 20*         | —           | 31          | 20           | —            |
| D GND        | 21*         | 21          | 30          | 21           | 21           |
| LRF_STB      | 22*         | —           | —           | —            | 22           |
| LFC_STB      | 23*         | —           | —           | 23           | —            |
| LIF_STB      | 24*         | —           | 27          | —            | —            |
| CAL OSC TUNE | 25          | 25*         | —           | —            | —            |
| LLOG_STB     | 26*         | 26          | —           | —            | —            |
| VCMON        | —           | —           | —           | 27           | —            |
| D GND        | 28*         | 28          | 23          | 28           | 28           |
| RT PULSE     | 29*         | —           | —           | —            | —            |
| HSCAN        | 30*         | —           | —           | 30           | —            |
| D GND        | 31*         | 31          | 20          | 31           | 31           |
| RESERVED     | —           | —           | —           | —            | —            |
| OFL ERR      | 33          | —           | —           | —            | 33*          |
| R/T DAC3     | 34*         | —           | —           | —            | —            |

\* Indicates signal source.

**Table 7-1. W2 Control Cable Connections (continued)**

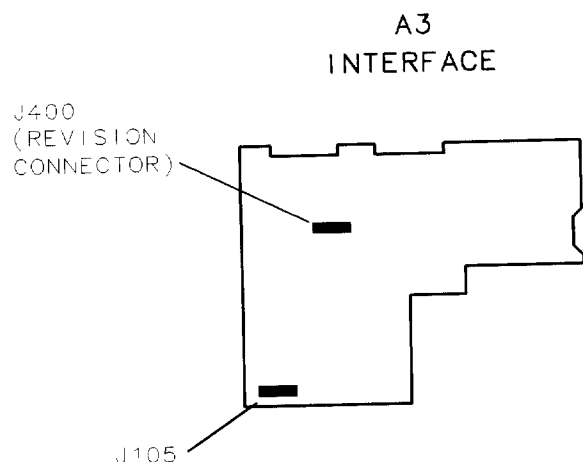
| Signal        | A3J2 (pins) | A4J2 (pins) | A5J2 (pins) | A14J2 (pins) | A15J2 (pins) |
|---------------|-------------|-------------|-------------|--------------|--------------|
| A GND         | 35*         | 35          | 16          | 35           | 35           |
| RF GAIN       | 36*         | —           | —           | —            | 36           |
| LO3 ERR       | —           | —           | —           | 37           | 37*          |
| A GND         | 38*         | 38          | 13          | 38           | 38           |
| LVFC_ENABLE   | 39*         | —           | —           | 39           | —            |
| FC ERR        | 40          | —           | —           | 40*          | —            |
| A GND         | 41*         | 41          | 10          | 41           | 41           |
| YTO ERR       | 42          | —           | —           | 42*          | —            |
| +10V REF      | 43*         | 43          | —           | —            | 43           |
| A GND         | 44*         | 44          | 7           | 44           | 44           |
| SCAN RAMP     | 45          | —           | —           | 45*          | —            |
| VIDEO TRIGGER | 46*         | —           | —           | —            | —            |
| A GND         | 47*         | 47          | 4           | 47           | 47           |
| NC            | —           | —           | —           | —            | —            |
| R/T DAC2      | 49*         | —           | —           | —            | —            |
| R/T DAC1      | 50*         | —           | —           | 50           | —            |

\* Indicates signal source.

## Troubleshooting Using the TAM

When using Automatic Fault Isolation, the TAM indicates suspected circuits that need to be manually checked. Use Table 7-2 to locate the manual procedure.

Table 7-3 lists assembly test connectors associated with each Manual Probe Troubleshooting test. Figure 7-1 illustrates the location of A3's test connectors.



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**Figure 7-1. A3 Test Connectors**

### Automatic Fault Isolation

Analog data bus errors that occur during Automatic Fault Isolation result from either a shorted W2 control cable or faulty A3 assembly. Perform the following steps to determine the cause of the error.

1. Disconnect W2 from A3J2 and repeat the Automatic Fault Isolation procedure.
2. If the analog data bus error is still present, troubleshoot the A3 Interface assembly. If the error disappears, look for a short on W2 or another assembly connecting to it.
3. To isolate a short on W2, reconnect W2 to A3J2 and disconnect W2 from all other assemblies.
4. Repeat the Automatic Fault Isolation routine.
5. If the analog data bus error is still present, W2 is shorted. If the error disappears, reconnect the other assemblies one at a time and repeat the procedure. Once the faulty assembly is reconnected to W2, the error should reappear.

**Table 7-2. Automatic Fault Isolation References**

| Suspected Circuit Indicated<br>by Automatic Fault Isolation | Manual Procedure to Perform                                                |
|-------------------------------------------------------------|----------------------------------------------------------------------------|
| Check ADC ASM                                               | ADC ASM                                                                    |
| Check ADC MUX                                               | ADC MUX                                                                    |
| Check ADC Start/Stop Control                                | ADC Start/Stop Control                                                     |
| Check Analog Bus Drivers                                    | Automatic Fault Isolation ( <i>in this chapter</i> )<br>Analog Bus Drivers |
| Check Analog Bus Timing                                     | Automatic Fault Isolation ( <i>in this chapter</i> )<br>Analog Bus Timing  |
| Check Interface Strobe Select                               | Interface Strobe Select                                                    |
| Check Keyboard Interface                                    | Keyboard/RPG Problems                                                      |
| Check Negative Peak Detector                                | Positive/Negative Peak Detectors<br>( <i>steps 3 through 10</i> )          |
| Check Peak Detector Reset                                   | Peak Detector Reset                                                        |
| Check Positive Peak Detector                                | Positive/Negative Peak Detectors<br>( <i>steps 3 through 10</i> )          |
| Check Real Time DAC                                         | Preselector Peaking Control (Real Time DAC)                                |
| Check Ramp Counter                                          | Ramp Counter                                                               |
| Check RF Gain DACs                                          | Band Flatness Control (RF Gain DACs)                                       |
| Check Rosenfell Detector                                    | Rosenfell Detector                                                         |
| Check RPG Interface                                         | Keyboard/RPG Problems                                                      |
| Check Track and Hold                                        | Track and Hold                                                             |
| Check Trigger                                               | Triggering Problems                                                        |
| Check Variable Gain Amplifier (VGA)                         | Variable Gain Amplifier (VGA)                                              |
| Check Video Filter                                          | Video Filter                                                               |
| Check Video Filter Buffer Amplifier                         | Video Filter Buffer Amplifier                                              |
| Check Video MUX                                             | Video MUX                                                                  |

**Table 7-3. TAM Tests versus A3 Test Connectors**

| Connector | Manual Probe Troubleshooting Test                                                                                                                                                                 | Measured Signal Lines                                                                               |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|
| A3J105    | Video Input to Interface<br>Video to Rear Panel<br>Video MUX<br>LOG Offset/LOG Expand<br>Video Filter Buffer Amp.<br>Video Peak Detectors<br>ADC MUX<br>Variable Gain Amplifier<br>Track and Hold | MS1<br>MS1, MS2<br>MS1, MS3<br>MS1, MS3<br>MS3, MS5, OS1<br>MS5, MS6<br>MS6<br>MS6, MS7<br>MS7, MS8 |
| A3J400    | Revision<br>Trigger<br>ADC Start/Stop Control<br>Video Trigger DAC<br>Real Time DAC #1<br>RF Gain DACs                                                                                            | MS2<br>MS8<br>MS7<br>MS1<br>MS3<br>MS6                                                              |

## Keyboard/RPG Problems

### Keyboard Interface

Refer to function block G of A3 Interface Assembly Schematic Diagram (sheet 3 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

A pressed key results in a low on a keyboard sense line (LKSNS0 through LKSNS7). This sets the output of NAND gate U607 high, generating KBD/RPG\_IRQ. The CPU determines the key pressed by setting only one keyboard scan line (LKSCN0 through LKSCN5) low through U602 and reading the keyboard sense lines.

1. If none of the keys or RPG responds, check ribbon cable, A1A1W1. (This cable connects the A1A1 keyboard to the A3 interface assembly.) The keys are arranged in a row/column matrix, as shown in Table 7-4.
2. If an entire row or column of keys does not respond, and the RPG does respond, there might be an open or shorted wire in A1A1W1.

**Table 7-4. Keyboard Matrix**

|        | LKSNS0         | LKSNS1         | LKSNS2 | LKSNS3     | LKSNS4 | LKSNS5         | LKSNS6 | LKSNS7         |
|--------|----------------|----------------|--------|------------|--------|----------------|--------|----------------|
| LKSCN0 | CONFIG         | SAVE           | RECALL | GHz        | MHz    | kHz            | Hz     | PRESET         |
| LKSCN1 | MODULE         | TRIG           | DISP   | 9          | 6      | 3              | BK SP  | ↑              |
| LKSCN2 | PEAK<br>SEARCH | BW             | TRACE  | 8          | 5      | 2              | •      | ↓              |
| LKSCN3 | FREQ<br>COUNT  | AUTO<br>COUPLE | MKR →  | 7          | 4      | 1              | 0      | HOLD           |
| LKSCN4 | SWEEP          | SK1            | SK2    | SK3        | SK4    | SK5            | SK6    | MKR            |
| LKSCN5 | AUX<br>CTRL    | MEAS/USER      | CAL    | SGL<br>SWP | COPY   | FRE-<br>QUENCY | SPAN   | AMPLI-<br>TUDE |

3. Check that all inputs to NAND gate A3U607 (LKSNS lines) are high when no key is pressed. If any input is low, continue with the following:
  - a. Disconnect A1A1W1 from A3J602 and again check all inputs to U607.
  - b. If any input is low with A1A1W1 disconnected, suspect A3U604, A3U607, or A3U602.
  - c. Reconnect A1A1W1 to A3J602.
4. Monitor A3U607 pin 8 with a logic probe. A TTL high should be present when any key is held down. Monitor this point while pressing each key in succession.
5. Check that the LKSCN lines (outputs of A3J602 pins 1 through 6) read a TTL low with no key pressed. (Any TTL high indicates a faulty A3 Interface assembly.)
6. Check that a pulse is present at each LKSCN output of U602 when a key is pressed.
7. Check that only one input to U607 (LKSNS lines) goes low when a key is pressed.
8. Check that U602 pin 9 (LKBD\_RESET) pulses low when a key is pressed.

9. If LKBD\_RESET is incorrect and a pulse is not present at each of the LKSCN outputs of U602 when a key is pressed, check for LWRCLK and LSCAN\_KBD.

## RPG Interface

Refer to function block J of A3 Interface Assembly Schematic Diagram (sheet 3 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

U608B latches the RPG direction from the two RPG outputs, RPG\_COUNT and RPG\_COUNT1. Counterclockwise RPG rotation produces low-going pulses which result in a high output on U608B. Clockwise RPG rotation results in a low output from U608B. U612A provides the edge to trigger one-shot U423B, which generates a 90 ms pulse. This pulse gates U610A for counting of RPG pulses by U606. Gates U610D and U614D prevent retriggering of U423B until its 90 ms pulse has timed out.

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**Note** Elsewhere, RPG\_COUNT1 is referred to as RPG\_01 and RPG\_COUNT is referred to as RPG\_02.

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1. Monitor A3U401 pin 2 with a logic probe or oscilloscope. Pulses should be present as the RPG is rotated.
2. Monitor A3U608 pin 12 as the RPG is rotated. Pulses should be present.
3. If pulses are missing at both points, check for power and ground signals to A1A1W1 and A1A2W1. If both power and ground are there, the A1A2 RPG is probably defective.
4. If pulses are missing at only one point, check for an open or short on A1A1W1 and A1A2W1. If these cables are working properly, A1A2 RPG is probably defective.
5. Press **LINE** to turn spectrum analyzer off and disconnect A1A1W1 from A3J602. Jumper A3U608 pin 12 (RPG\_COUNT) to U608 pin 14 (+5 Vdc). Jumper U401 pin 2 (RPG\_COUNT1) to U511 pin 11 (HDPKD\_CLK). This provides a 7.8 kHz square wave to the RPG\_COUNT1 input of the RPG Interface.
6. Press **LINE** to turn spectrum analyzer on.
7. Check A3U608 pin 9 for narrow, low-going pulses approximately every 90 ms.
8. Check A3U608 pin 13 (LRPG\_RESET) for narrow, low-going pulses approximately every 90 ms.
9. Check A3U612 pin 5 for narrow, low-going pulses approximately every 90 ms.
10. Check U608 pin 5 (HRPG\_IRQ) for narrow, high-going pulses approximately every 90 ms.
11. If HRPG\_IRQ is correct but LRPG\_RESET is incorrect, check U505 pin 13 (LKBD/RPG\_IRQ) for narrow, low-going pulses approximately every 90 ms.
12. If HRPG\_IRQ and LKBD/RPG\_IRQ are correct but LRPG\_RESET is incorrect, suspect a failure on the A2 controller assembly.
13. Check U610 pin 3 for a 7.8 kHz square wave. Check U606 pin 2 (HRPG\_RESET) for narrow, high-going pulses approximately every 90 ms. Refer to Table 7-5 and check the frequencies at divide-by-16 counter A3U606.
14. If all the checks above are correct but the spectrum analyzer does not respond to the RPG, suspect a problem in either the A1A2 RPG or the A1A1 Keyboard.

15. Press **LINE** to turn spectrum analyzer off.
16. Reconnect A1A1W1 to A3J602 and remove all jumpers.

**Table 7-5. Counter Frequencies**

| A3U606 pin # | Nominal Frequency (Hz) |
|--------------|------------------------|
| 3            | 3900                   |
| 4            | 1950                   |
| 5            | 975                    |
| 6            | 488                    |
| 11           | 244                    |
| 10           | 122                    |
| 9            | 61                     |

## Triggering or Video Gating Problems

Refer to function block H of A3 Interface Assembly Schematic Diagram (sheet 3 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The 1 MHz ADC clock provides synchronization in FREE RUN and SINGLE triggering. LINE triggering synchronization originates on the A6 power supply. Trigger MUX A3U613 selects between FREE RUN, VIDEO, LINE, and EXTERNAL trigger sources. The trigger signal sets the output of the HSCAN latch high. HBADC\_CLK0 provides the trigger signal for FREE RUN. The VIDEO TRIG signal must be at least 25 mV (0.25 divisions) peak-to-peak to trigger in video trigger mode.

The trigger for Gated Video has two modes of operation, level mode and edge mode. In the edge mode, positive-edge or negative-edge triggering can be selected. Output 0 from pin 10 of A3U617 generates the gate delay and output 1 from pin 13 of A3U617 generates the gate length. The duration of these two time intervals is set using front-panel softkeys under the **SWEEP** key. The trigger input for Gated Video is the rear-panel EXT/GATE TRIG INPUT (TTL > 10 k $\Omega$ ).

1. Check that the trigger MUX is receiving the proper trigger source information by selecting each of the following trigger modes and checking the TRIG\_SOURCE0 and TRIG\_SOURCE1 lines as indicated in Table 7-6.
2. If a trigger mode does not work, check that a trigger signal is present at the appropriate trigger MUX input, as indicated in Table 7-6.

**Table 7-6. Trigger MUX Truth Table**

| Trigger Mode | TRIG_SOURCE0<br>U613 pin 14 | TRIG_SOURCE1<br>U613 pin 2 | MUX Input<br>Pin Number U613 |
|--------------|-----------------------------|----------------------------|------------------------------|
| FREE RUN     | L                           | L                          | 6                            |
| VIDEO        | H                           | L                          | 5                            |
| LINE         | H                           | H                          | 3                            |
| EXTERNAL     | L                           | H                          | 4                            |

3. Check that the appropriate trigger MUX input signal is present at the trigger MUX output (A3U613 pin 7).
4. To check the video trigger level DAC, connect a DVM's positive lead to A3J400 pin 1 and the negative DVM lead to A3TP4.
5. Press **TRIG** and **VIDEO**.
6. Press the STEP **▼** key several times while noting the DVM reading and position of the video trigger level on the screen.
7. Check that the voltage displayed on the DVM changes by 1 V for each step of the VIDEO TRIG LEVEL.
8. If the voltage changes incorrectly, proceed as follows:
  - a. Check the -10 Vdc reference (A3U409 pin 4).
  - b. While using the front-panel knob to adjust the video trigger level, check for the presence of pulses on A3U409 pin 15 (LDAC2).
  - c. While using the front-panel knob to adjust the video trigger level, check for the presence of pulses on A3U409 pin 16 (LWRCLK).
  - d. Check that pulses are present on U409 pin 6 (IA0).
9. If the LWRCLK and LDAC2 signals are not correct, refer to "Interface Strobe Select" in this chapter.
10. If correct trigger pulses are present at the trigger MUX output (A3U613 pin 7), but the instrument does not appear to be sweeping, proceed as follows:
  - a. Press **PRESET**, **SWEEP**, and **DLY SWP ON OFF** until ON is underlined, then **DLY SWP [ ]** 30 milliseconds.
  - b. Using an oscilloscope, check for activity at pins 1 and 3 of A3U615A.
  - c. If there is activity at pin 1 but not at pin 3 of A3U615A, suspect A3U616 or A3U617.
  - d. If there is activity at pin 1 and pin 3 of A3U615A, suspect A3U615. (Check pin 5 for activity.)
11. If there is a problem with Video Gating, proceed as follows:
  - a. Press **PRESET** and set the HP 8560E as follows:
 

|                  |       |         |
|------------------|-------|---------|
| Center frequency | ..... | 300 MHz |
| Span             | ..... | 0 Hz    |
| Sweep time       | ..... | 150 ms  |
  - b. Press **TRIG**, **EXTERNAL**, then **SWEEP** and **GATE ON OFF** until ON is underlined.
  - c. Press **GATE DLY [ ]** 10 milliseconds, then press **GATE LEN [ ]** 30 milliseconds.
  - d. Connect a pulse/function generator (such as an HP 8116A) to provide a 5 V peak-to-peak square wave (TTL level) to the HP 8560E rear-panel EXT/GATE TRIG INPUT and also (using a BNC tee) to the channel 4 input of the oscilloscope (HP 54501A).
  - e. Set the pulse/function generator to NORMAL mode with a duty cycle of 50% and a frequency of 10 Hz.

f. Press the following keys on the oscilloscope:

**CLEAR DISPLAY**

off frame axes grid ..... highlight **grid**  
connect dots off on ..... highlight **on**

**TRIG**

source 1 2 3 4 ..... highlight **4**  
level ..... 2 V

**TIMEBASE**

**TIMEBASE** ..... 50 ms/div

**CHAN**

**CHANNEL 1 2 3 4 off on**

highlight **CHANNEL 1 on**

set V/div to 0.2 V and offset to 0.6 V (10:1 probe used)

highlight **CHANNEL 4 on**

set V/div to 2 V and offset to 0 V

**DISPLAY**

**DISPLAY norm avg env** ..... highlight **norm**

- g. Using a 10:1 probe connected to channel 1 of the oscilloscope, check for activity at pins 10 and 13 of A3U617.
- h. If either pin (or both) show no activity, check for activity at pin 21 (LTIMER) of A3U617.
- i. If LTIMER is not active, troubleshoot the Interface Strobe Select circuitry (block K)
- j. If there was activity at pins 10 and 13 of A3U617, suspect A3U616.

## Preselector Peaking Control (Real Time DAC)

Refer to function block L of A3 Interface Assembly Schematic Diagram (sheet 4 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The HP 8560E uses a real-time DAC (R/T DAC1) to peak the preselector.

1. Press **PRESET** on the HP 8560E and set the span to 0 Hz.
2. Connect a positive DVM lead to A3J400 pin 3 and the negative DVM lead to A3TP4.
3. Press **MKR**, **AUX CTRL**, **INTERNAL MIXER**, and **PRESEL MAN ADJ**.
4. Monitor the DVM reading while changing the PRESELECTOR TUNE value from 0 to 255. The PRESELECTOR TUNE value is R/T DAC1's setting.
5. Check that the DVM reading increases from 0 to approximately +10 Vdc as R/T DAC1 is set from 0 to 255.
6. If the voltage does not change as described, set the spectrum analyzer to single trigger mode and check the following:
  - a. Check that A3U409B pin 18 is at -10 Vdc.

- b. Check for the presence of pulses at U409 pin 6 (IA0).
  - c. Check that pulses are present at U409 pin 15 (LDAC2).
  - d. Check that pulses are present at U409 pin 16 (LWRCLK).
7. If the LDAC2 or LWRCLK signals are incorrect, refer to “Interface Strobe Select” in this chapter.

## Flatness Control (RF Gain DACs)

Refer to function block M of A3 Interface Assembly Schematic Diagram (sheet 4 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

RF Gain DACs control the A15 assembly's flatness compensation amplifiers. The RF Gain DACs are arranged so that the output of one DAC is the voltage reference for the other DAC. This results in an RF GAIN voltage which is exponentially proportional to the DAC settings. Each DAC is set to the same value. The A15 RF assembly converts the RF GAIN signal to a current for driving the PIN diode attenuators in the Flatness Compensation Amplifiers. The exponentially-varying voltage compensates for the nonlinear resistance-versus-current characteristic of the PIN diodes.

1. Place the WR PROT/WR ENA jumper on the A2 controller assembly in the WR ENA position.
2. Press **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **FLATNESS**, and **FLATNESS DATA**. Press **NEXT BAND** until “FLATNESS BAND # 0” is displayed.
3. Press the **▲** key until “DATA @ 300 MHz” is displayed. Note the number directly below “DATA @ 300 MHz”; this is the RF Gain DAC value.
4. Connect a positive DVM lead to A3J400 pin 13 and the negative DVM lead to A3TP4.
5. Check that the DVM reading increases from near 0 Vdc to between -1.3 and -1.9 Vdc as the RF Gain DAC setting is increased from 0 to 4095.
6. If the DVM readings are incorrect, press **PRESET**, **SGL SWP**, **CAL**, **MORE 1 OF 2**, **SERVICE CAL DATA**, **FLATNESS**, and **FLATNESS DATA**. Press **NEXT BAND** until “FLATNESS BAND # 0” is displayed. Press the **▲** key until “DATA @ 300 MHz” is displayed. Proceed as follows:
  - a. Check the +10 V reference.
  - b. Check for narrow, low-going pulses at A3U417 pin 13 (LWRCLK).
  - c. While rotating the front-panel knob, check for narrow, low-going pulses at A3U417 pin 1 (LDAC1) and pin 14 (LDACU1).
  - d. While rotating the front-panel knob, check for narrow, low-going pulses at U417 pin 16 (L-IA0) and pin 15 (IA4).
7. If the LWRCLK, LDAC1, or LDACU1 is incorrect, refer to the Interface Strobe Select block in this chapter.
8. Place the WR PROT/WR ENA jumper on the A2 controller assembly in the WR PROT position. Press **PRESET**.

## A3 Assembly's Video Circuits

Voltages from A3J101 to A3's Variable Gain Amplifier correspond (approximately) to on-screen signal levels. (One volt corresponds to the top of the screen and zero volts corresponds to the bottom of the screen.) This is true for both log and linear settings except when the spectrum analyzer is in 1 dB/div or 2 dB/div. In these cases the log expand amplifier is selected, and 1 V corresponds to top-screen and 0.8 or 0.9 V corresponds to bottom-screen. The spectrum analyzer can be set to zero span at the peak of a signal to generate a constant dc voltage in the video circuits during sweeps.

1. Disconnect W26 from A3J101 and W20 from A2J4.
2. Connect W26 to A2J4.
3. Set the HP 8560E to the following settings:

|                            |           |
|----------------------------|-----------|
| Span .....                 | 0 Hz      |
| Sweep time .....           | 20 ms     |
| Resolution bandwidth ..... | 1 MHz     |
| Log/division .....         | 10 dB/div |
4. If a trace is displayed, troubleshoot the A3 assembly. If a trace is absent, connect an oscilloscope to the rear-panel BLKG/GATE OUTPUT.
5. The presence of a TTL signal (TTL low during 20 ms sweep) indicates a good A3 Interface Assembly. Troubleshoot the IF section.
6. If the BLKG/GATE OUTPUT is always at a TTL high or low, troubleshoot the A3's trigger/video gating circuits.
7. Reconnect W26 to A3J101 and W20 to A2J4.
8. Remove the A3 assembly's shield.
9. If the video filters appear to be faulty, refer to "Video Filter" in this chapter.
10. If there appears to be a peak detector problem, refer to "Positive/Negative Peak Detectors" in this chapter.
11. Connect the HP 8560E's CAL OUTPUT to the INPUT 50 $\Omega$  and set the controls as follows:

|                        |         |
|------------------------|---------|
| Center frequency ..... | 300 MHz |
| Span .....             | 0 Hz    |
| Reference level .....  | -10 dBm |
12. If the spectrum analyzer works correctly in 5 dB/div and 10 dB/div but not in 1 dB/div or 2 dB/div, refer to "Log Offset/Log Expand" in this chapter. Continue with step 13 if the problem involves on-screen amplitude errors which appear to originate in the video chain.
13. Press **CAL** and **IF ADJ ON OFF** until OFF is underlined. Monitor A3TP9 with an oscilloscope. If the voltage is not approximately +1 Vdc, troubleshoot the Log Amplifier on A4. (Refer to the IF troubleshooting procedure in Chapter 8.)
14. To confirm proper video input to the video circuit, set the HP 8560E to Log 10 dB per division and change the reference level in 10 dB steps from -10 dBm to +30 dBm. At each 10 dB step, the input voltage should change 100 mV. The input level should be +0.6 Vdc for a +30 dBm reference level.

**Note**

The on-screen amplitude level will probably not change as expected, since the video circuitry is assumed to be faulty.

15. Monitor A3TP14 while stepping the reference level from  $-10$  dBm to  $+30$  dBm. If the voltage does not step approximately 100 mV per 10 dB step, refer to "Video MUX" in this chapter.
16. If the Video MUX is working properly, monitor A3TP15 with the oscilloscope and step the reference level from  $-10$  dBm to  $+30$  dBm. If the voltage does not change 100 mV per 10 dB step, refer to "Video Filter" in this chapter.
17. If the voltage at A3TP15 is correct, move the oscilloscope probe to A3TP17 and step the reference level between  $-10$  dBm and  $+30$  dBm. If the voltage does not change 100 mV per 10 dB step, refer to "Video Filter Buffer Amplifier" in this chapter.
18. If the voltage at A3TP17 is correct, move the oscilloscope probe to A3TP6. Set the following controls to keep the ADC MUX set to the MOD\_VIDEO input during the sweep.  
SWEEP TIME ..... 50 s  
DETECTOR MODE ..... SAMPLE
19. Step the reference level from  $-10$  dBm to  $+30$  dBm while monitoring the voltage change on the oscilloscope. If the voltage does not change 100 mV per 10 dB step, refer to "ADC MUX" in this chapter.
20. If the voltage at A3TP6 is correct, move the oscilloscope probe to A3TP8 and step the reference level between  $-10$  dBm and  $+30$  dBm. If the voltage at A3TP8 is not the same as that at A3TP6, replace A3U110.
21. If the voltage at A3TP8 and A3TP6 are equal, move the oscilloscope probe to A3TP7.
22. Change the reference level from  $-10$  dBm to 0 dBm. The voltage change on A3TP7 should be between 630 mV and 770 mV. If the voltage change is outside of these limits, refer to "Variable Gain Amplifier (VGA)" in this chapter. The gain of the VGA should be  $7 \pm 10\%$ .

**Log Offset/Log Expand**

Refer to function block X of A3 Interface Assembly Schematic Diagram (sheet 5 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The log scales are modified using a combination of amplification and digital trace manipulation. The video input to the A3 assembly is either 10 dB/div or linear. To obtain the 5 dB/div scale, the CPU manipulates the trace data from the 10 dB/div scale. To obtain the 2 dB/div scale, the video signal is amplified and offset so that top-screen in 10 dB/div corresponds to top-screen in 2 dB/div. To obtain the 1 dB/div scale, the CPU manipulates trace data from the 2 dB/div scale.

In 2 dB/div, Log Offset/Log Expand amplifies the top 20 dB of the display. This is done by offsetting the video signal by  $-0.8$  V and providing a gain of 5 to the top 0.2 V of the video signal. The  $-0.8$  V offset is accomplished by sinking 2 mA through R114 by current source U105/Q101.

1. On the HP 8560E, press **PRESET**, **SPAN**, **ZERO SPAN**, **CAL**, and **IF ADJ OFF**.

2. Disconnect W26 (coax 2) from A3J101 and connect the output of a function generator to A3J101.

3. Set the function generator to the following settings:

Output ..... Sine wave  
Amplitude ..... 1 V pk-to-pk  
DC Offset ..... +500 mV  
Frequency ..... 50 Hz

4. Set the HP 8560E sweep time to 50 ms.

5. Adjust the function generator amplitude and offset until the sine wave fills the entire graticule area.

6. Measure and note the function generator's peak-to-peak voltage using an oscilloscope.

$$V_{(10 \text{ dB/div})} = \text{_____ V}$$

7. Set the HP 8560E to 2 dB/div.

8. Readjust the function generator amplitude and offset until the sine wave again fills the entire graticule area.

9. Measure the function generator's peak-to-peak voltage and dc offset.

$$V_{(2 \text{ dB/div})} = \text{_____ V}$$

10. The ratio of voltage recorded in step 6 to the voltage recorded in step 9 should be  $5 \pm 3\%$ .  
If the ratio is not 5, troubleshoot the A3 Interface assembly.

11. Reconnect W26 to A3J101.

## Video MUX

Refer to function block U of A3 Interface Assembly Schematic Diagram (sheet 5 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

1. Press **PRESET** and set the HP 8560E controls as follows:

Center frequency ..... 300 MHz  
Span ..... 0 Hz

2. Press **SGL SWP**, **CAL**, and **IF ADJ OFF**. Connect the CAL OUTPUT to the INPUT 50Ω connector.

3. Check for a TTL high on A3U104 pin 2 and a TTL low on U104 pin 10. Set the spectrum analyzer to 2 dB/div and check for a TTL high on A3U104 pin 10 and a TTL low on A3U104 pin 2.

4. If the logic levels on A3U104 are incorrect, check the LLOG\_STB signal as follows:

a. Monitor A3U104 pin 9 with an oscilloscope or logic probe. Check that a 1 microsecond, low-going pulse is present when switching between 10 dB/div and 2 dB/div.

b. Check the inputs to A3U104 (pins 3 and 11) while switching between 10 dB/div and 2 dB/div.

- c. If the logic signals are incorrect, refer to "Analog Bus Timing" and "Analog Bus Drivers" in this chapter.
5. Check comparators A3U109A/C for proper outputs. The outputs should be high when the noninverting input is greater than the threshold voltage of +1.3 Vdc.
6. If A3U104 and A3U109 are working properly, set the **AMPLITUDE** and **REF LVL** to 0 dBm.
7. Monitor the voltage at A3TP14 while switching the spectrum analyzer between 10 dB/div and 2 dB/div. The voltage should switch between 0.8 and 0.4 Vdc.
8. If the voltage at A3TP14 is incorrect, suspect either A3Q220 or A3Q221.
9. The Video MUX will appear faulty if A3CR109 is shorted or leaky. Diode A3CR109 clamps the voltage at A3TP14 to -0.4 V when in log expand with less than 0.8 V at J101. To confirm this failure, lift diode A3CR109's cathode and perform steps 1 through 7 again.
10. To return the HP 8560E to automatic sweep, press **SWEEP**, **SWEEP CONT SGL** or press **PRESET**.

## Video Filter

Refer to function block V of A3 Interface Assembly Schematic Diagram (sheet 5 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The HP 8560E uses digital filtering for 1 Hz to 100 Hz video bandwidths. An RC low-pass filter is used for 300 Hz to 3 MHz video bandwidths. Various series resistances and shunt capacitances switch into the video filter to change its cutoff frequency.

When Gated Video is selected, the video signal is "gated" (turned on periodically for a set duration of time). This function is shown in

block V of the block diagram as a series switch that allows the video signal to pass only when it is closed. The actual switch, U109B/CR118, shunts the video to ground (video signal is passed only when the switch is open). The control circuitry for this switch is described under "Triggering or Video Gating Problems" in this chapter. The rear-panel EXT/GATE TRIG INPUT provides the connection for triggering in the Gated Video mode. The gate output signal is available at the rear-panel BLKG/GATE OUTPUT connector. Positive or negative edge mode, or level mode can be selected from the front panel.

1. Press **PRESET** and set the HP 8560E controls to the following settings:

|                  |                       |
|------------------|-----------------------|
| Center frequency | ..... 225 MHz         |
| Span             | ..... 550 MHz         |
| Sweep time       | ..... Uncoupled (MAN) |

2. Press **CAL** and **IF ADJ OFF**.
3. Step the Video BW from 3 MHz to 10 kHz. At each step, the peak-to-peak deviation of the noise should decrease.
4. Step the Video BW down to 1 Hz. At each step, the amplitude of the LO feedthrough should decrease.
5. Refer to Table 7-7 and check for correct latched levels for the selected video bandwidth setting.

6. If latch A3U102's output is not correct, trigger an oscilloscope on LLOG\_STB (U102 pin 9) and monitor U102 pin 1 and other latch inputs while changing the video bandwidth.
7. If the inputs are incorrect, troubleshoot the analog bus. Correct inputs with bad outputs indicate a faulty U102.
8. Check that the outputs of A3U111A, A3U111B, and A3U107A/B/C/D are correct for their inputs. The outputs should be high with noninverting inputs higher than the +1.4 V threshold voltage. If a voltage drop is noticed across these components, suspect A3CR109 or A3Q317B. Since no dc current flows through any of the series resistances or FETS (drain to source), no voltage drops should occur.
9. To return the HP 8560E to automatic sweep, press **SWEEP**, **SWEEP CONT SGL** or **PRESET**.

**Table 7-7. A3U102 Latch Outputs**

| Video BW | Pin 2 | Pin 5 | Pin 7 | Pin 10 | Pin 12 | Pin 15 |
|----------|-------|-------|-------|--------|--------|--------|
| 300 Hz   | H     | L     | L     | L      | L      | L      |
| 1 kHz    | L     | L     | L     | L      | L      | H      |
| 3 kHz    | L     | H     | L     | L      | L      | L      |
| 10 kHz   | L     | L     | L     | L      | H      | L      |
| 30 kHz   | H     | L     | H     | L      | L      | L      |
| 100 kHz  | L     | L     | H     | L      | L      | H      |
| 300 kHz  | L     | H     | H     | L      | L      | L      |
| 1 MHz    | L     | L     | H     | L      | H      | L      |
| 3 MHz    | L     | L     | L     | H      | L      | L      |

## Video Filter Buffer Amplifier

Refer to function block W of A3 Interface Assembly Schematic Diagram (sheet 5 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The video filter buffer amplifier provides outputs for video trigger, positive and negative peak detectors, and the analog zero-span (sweeps <30 ms). The zero-span video output is terminated in 500 ohms on the A2 Controller assembly. The amplifier is a high-input-impedance buffer amplifier with a gain of one when properly terminated.

Current source U307C provides twice the current of Q316. Resistor R145 and current source U307D shift the dc level. Resistor R260 terminates the peak detector inputs in 500 ohms. The unterminated gain is 1.1. Diode CR114 prevents latchup during positive overdrive conditions while CR113 protects Q318 during overdrive. Diode CR117 is a 12.7 V zener that limits the peak detector's output to +1.5 V. Typically, limiting occurs at +1.1 V.

## Positive/Negative Peak Detectors

Refer to function blocks Y and Z of A3 Interface Assembly Schematic Diagram (sheet 5 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The following information pertains to the positive peak detector and is applicable to troubleshooting the negative peak detector.

The positive peak detector consists of an input amplifier (A3U204 and A3Q210) followed by detector diodes (A3CR203 and A3CR204) and hold capacitor A3C217. Output amplifier A3Q206, Q211, and Q212 buffers the hold capacitor. Both the input and output amplifiers have a gain of one. Each amplifier has local feedback. On the output amplifier the emitter of Q212 connects to Q206's gate. On the input amplifier the feedback goes through Q209 and Q208 back to the base of U204D. Global feedback occurs from the output amplifier through R223 back to the input amplifier U204D. The peak detector resets through Q207.

1. Press **PRESET** and set the HP 8560E controls as follows:

|                      |           |
|----------------------|-----------|
| Center frequency     | 300 MHz   |
| Span                 | 500 MHz   |
| Resolution bandwidth | AUTO      |
| Video bandwidth      | AUTO      |
| Log dB/division      | 10 dB/div |

2. If the HP 8560E does not meet the conditions in steps a through e below, the positive and negative peak detectors are probably faulty. Continue with step 3 to check the detectors.
  - a. The peak-to-peak deviation of the noise in NORMAL detector mode should be approximately two divisions. Press **TRACE**, **TRACE B**, **CLEAR WRITE B**, **VIEW B**, **TRACE A**, **MORE 1 of 3**, and **DETECTOR MODES**.
  - b. Select **DETECTOR POS PEAK** mode.
  - c. Confirm that the noise is about one-third division peak-to-peak. The noise should also be no higher than the top of the noise level in NORMAL detector mode.
  - d. Select **DETECTOR NEG PEAK** mode. The noise should be about one-third of a division peak-to-peak. The noise should also be no lower than the bottom of the noise in NORMAL mode.
  - e. Select **DETECTOR SAMPLE** mode. Check that the noise appears between the top and bottom of the noise in NORMAL mode.
3. On the HP 8560E, connect the front-panel CAL OUTPUT to the INPUT 50 $\Omega$  and set the controls to the following settings:

|                  |          |
|------------------|----------|
| Center frequency | 300 MHz  |
| Span             | 0 Hz     |
| Sweep time       | 5 s      |
| Detector mode    | POS PEAK |
4. Monitor A3TP17 and A3TP16 simultaneously with an oscilloscope.
5. Change the reference level from -10 dBm to +30 dBm and verify a voltage change at both A3TP17 and A3TP16 of 0.9 V to 0.5 V in 100 mV steps.
6. Check the entire range of the detector by substituting a dc source at J101 and varying its output from 0 V to 1 V.

7. If the peak detector appears latched up, check LPOS\_RST (U422 pin 4) for a negative TTL level reset pulses. The reset pulses should occur every 130  $\mu$ s and should be approximately 250 ns wide.
8. If the reset pulses are absent, troubleshoot the Peak Detector Reset circuitry.
9. If the reset pulses are present, check the gate of Q207. The pulses should be positive-going from -12.7 V to -1.35 V.
10. The peak detector can be made into a unity gain amplifier by shorting the cathode of CR203 to the anode of CR204. If the peak detector functions normally as a unity gain amplifier, suspect Q208 or CR203 or CR204.

### Peak Detector Reset

Refer to function block R of A3 Interface Assembly Schematic Diagram (sheet 4 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

1. Press **PRESET** on the HP 8560E and set the controls as follows:
 

|                  |                |
|------------------|----------------|
| Center frequency | .....300 MHz   |
| Span             | ..... 0 Hz     |
| Sweep time       | ..... 5 s      |
| Detector mode    | ..... POS PEAK |
2. Check that HHOLD (A3U526 pin 11) has 18  $\mu$ s wide pulses every 128  $\mu$ s.
3. Check that HODD (U408 pin 5) is a square wave with a period of 16.7 ms (2  $\times$  sweep time/600).
4. Check LPOS\_RST (U422 pin 4) for 200 ns low-going pulses every 128  $\mu$ s.
5. Check LNEG\_RST (A3U422 pin 12) for 200 ns low-going pulses every 128  $\mu$ s.
6. Set the detector mode to NORMAL and check that LNEG\_RST (A3U422 pin 12) has two pulses spaced 40  $\mu$ s apart and then a single pulse approximately 88  $\mu$ s from the second pulse.
7. Check HMUX\_SEL0 (A3U408 pin 3) and HMUX\_SEL1 (A3U408 pin 9) according to Table 7-8.

**Table 7-8. HMUX\_SEL0/1 versus Detector Mode**

| Detector Mode | HMUX_SEL0 (U408 pin 3)             | HMUX_SEL1 (U408 pin 9)             |
|---------------|------------------------------------|------------------------------------|
| NORMAL        | 15 $\mu$ s pulse every 128 $\mu$ s | 40 $\mu$ s pulse every 128 $\mu$ s |
| SAMPLE        | H                                  | H                                  |
| POS PEAK      | H                                  | L                                  |
| NEG PEAK      | L                                  | H                                  |

## Rosenfell Detector

Refer to function block S of A3 Interface Assembly Schematic Diagram (sheet 4 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

If both HPOS\_HLDNG and HNEG\_HLDNG are high during the same bucket, HROSENFELL will also be set high. This indicates that the video signal probably consists of noise, since it rose and fell during the same period. The HROSENFELL signal is valid only when the NORMAL (rosenfell) detector mode is selected.

1. Remove anything connected to the HP 8560E front-panel INPUT 50 $\Omega$  connector. Press

**PRESET** on the HP 8560E and set the controls as follows:

|                  |              |
|------------------|--------------|
| Center frequency | .....300 MHz |
| Span             | ..... 0 Hz   |
| Sweep time       | ..... 5 s    |
| Detector mode    | ..... NORMAL |

2. Check LPOS\_RST and LNEG\_RST as described in "Peak Detector Reset."
3. Check A3U423 pin 4 for two low-going 3.3  $\mu$ s pulses 40  $\mu$ s apart occurring every 130  $\mu$ s.
4. Check that HROSENFELL (A3U610 pin 6) has two pulses spaced approximately 40  $\mu$ s apart and then a third pulse 60  $\mu$ s from the second pulse. Each pulse should be approximately 10  $\mu$ s wide and low-going.
5. Monitor HROSENFELL with an oscilloscope while reducing the video bandwidth from 1 MHz to 1 kHz.
6. As the video bandwidth is decreased to 1 kHz, the HROSENFELL line should increasingly show a low logic level. With a video bandwidth of 1 kHz, a nearly flat line should be displayed on the CRT.
7. Set the sweep time to 50 ms. Externally trigger the oscilloscope using the HP 8560E rear-panel BLKG/GATE OUTPUT.
8. Check that HPOS\_HLDNG (A3U416 pin 4) is mostly high with a 1 MHz video bandwidth and mostly low with a 1 kHz video bandwidth.
9. Check that HNEG\_HLDNG (U416 pin 9) is mostly high with a 1 MHz video bandwidth and mostly low with a 1 kHz video bandwidth.

## ADC MUX

Refer to function block AA of A3 Interface Assembly Schematic Diagram (sheet 6 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The ADC MUX switches various inputs into the video path for conversion by the ADC. The SCAN RAMP input is used during sweeps having a width of equal to or greater than 2.01 MHz times N, to control the timing of the ADC operations. Some combination of MOD\_VIDEO, NEG\_PEAK, and POS\_PEAK is used for the video signal to be converted by the ADC. The YTO ERR, FCMUX, CAL OSC TUNE, and OFL ERR inputs are used only during diagnostic and auto adjust routines and during retrace.

1. Set the HP 8560E to the following settings:

Center frequency ..... 300 MHz  
Span ..... 0 Hz  
Reference level ..... -10 dBm  
Sweep time ..... 50 s  
DETECTOR MODE ..... SAMPLE

2. Refer to Table 7-9 and check for correct logic levels at A3U108 pins 1, 15, and 16. Check for proper output signals at TP6. If the select lines are not changing, suspect the ADC ASM or the VGA/ADC MUX Control. If the select lines are changing, but the proper video inputs are not being switched to the output, replace U108. In SAMPLE mode, the input is MOD\_VIDEO (pin 7); in POS PEAK mode, the input is POS\_PEAK (pin 5); and in NEG PEAK mode, the input is NEG\_PEAK (pin 6).
3. Check for the presence of the YTO ERR signal at A3J2 pin 42 with an oscilloscope probe.
4. If ERR 300 YTO UNLK or 301 YTO UNLK occurs and the voltage is near zero during a sweep and positive during retrace (YTO is being locked), the fault is on the A3 assembly. If a constant dc voltage is present, refer to the Synthesizer section troubleshooting procedure in Chapter 10.

**Table 7-9. Logic Levels at A3U108**

| Detector Mode | U108 pin 1 | U108 pin 15 | U108 pin 16 |
|---------------|------------|-------------|-------------|
| SAMPLE        | H          | L           | H           |
| POS PEAK      | H          | L           | L           |
| NEG PEAK      | L          | L           | H           |

5. Set the HP 8560E to the following settings:  
Span ..... 5 MHz  
Sweep time ..... 50 ms
6. Check for the presence of the SCAN RAMP signal by connecting an oscilloscope probe to A3J2 pin 45 (component side of A3J2). Connect the negative-probe lead to A3TP4.
7. A 0 to 10 V ramp should be present in both LINE and FREE RUN trigger modes. If the waveform is present only in LINE trigger, ADC control signal HBADC\_CLK0 may be faulty. Refer to "ADC Control Signals" in this chapter.
8. If the scan ramp is present, but is not being switched to the output of U108, replace U108. If the scan ramp is absent in either mode, do the following:
  - a. Connect the oscilloscope probe to A3J400 pin 15 (HSCAN).
  - b. A TTL signal (high during 50 ms sweep time and low during retrace) should be present, indicating A3 is working properly. Refer to the Synthesizer section troubleshooting procedure in Chapter 10. A faulty TTL signal indicates a bad A3 Interface assembly.
9. Set the HP 8560E to the following settings:  
Sweep time ..... 100 ms  
Span ..... 100 MHz

10. Press **CAL** and **IF ADJ ON** and check for the presence of the CAL OSC TUNE signal by monitoring A3J401 pin 25 with an oscilloscope. If ERR 499 CAL UNLK is displayed and a signal within the range of  $-10\text{ V}$  to  $+10\text{ V}$  is present during part of the retrace period, the fault is on the A3 assembly.
11. If a constant dc voltage is present during the sweep and all of the retrace period, refer to the IF Section troubleshooting procedure in Chapter 8.

### Variable Gain Amplifier (VGA)

Refer to function block AB of A3 Interface Assembly Schematic Diagram (sheet 6 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The VGA provides adjustable gain in the video path. Its nominal gain of 7 can be adjusted  $\pm 10\%$ . U112 removes dc offset to keep U113 in its monotonic range. (Both U112 and U113 are set to the same value.) The DAC settings cannot be changed from the front panel.

### Track and Hold

Refer to function block AC of A3 Interface Assembly Schematic Diagram (sheet 6 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

1. Press **PRESET** on the HP 8560E and set the controls as follows:

|                  |       |                  |
|------------------|-------|------------------|
| Center frequency | ..... | 300 MHz          |
| Span             | ..... | 0 Hz             |
| Detector mode    | ..... | Sample           |
| Reference level  | ..... | $-70\text{ dBm}$ |
| Log dB/division  | ..... | 2 dB/div         |
| Sweep time       | ..... | 50 ms            |

2. Disconnect any signal from the spectrum analyzer input. A full scale display of sampled noise should be present.
3. Trigger an oscilloscope on the positive going edge of HHOLD (A3U506 pin 16).
4. The waveform at A3TP10 should be random noise with an average level of approximately 4 V. The noise should have a flat spot in its response while HHOLD is high, indicating proper operation of U114.

## A3 Assembly's ADC Circuits

The ADC consists of a 12-bit DAC, 12-bit successive approximation register (SAR), data multiplexers, and data latches. The ADC ASM (algorithmic state machine) controls the ADC. Eight inputs are controlled by the ADC MUX. These include a positive peak detector, negative peak detector, sampled video, scan ramp, YTO error voltage, FC MUX voltages, Cal Oscillator tune voltage, and offset lock error voltage. A MUX on the A14 frequency control assembly selects which voltage is sent to the ADC MUX on the FC MUX signal line.

During NORMAL detector mode sweeps, when noise is detected by the rosenfell detector, the ADC ASM automatically switches between POS PEAK and NEG PEAK.

### ADC Control Signals

Refer to function blocks B and F of A3 Interface Assembly Schematic Diagram (sheet 2 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The ADC requires two signals from the A2 controller assembly: HBADC\_CLK0 and HBBKT\_PULSE. HBBKT\_PULSE is used only in zero span. Use the following steps to verify the signals.

1. Disconnect W22 from A2J8.
2. If a 10 MHz TTL signal is absent on W22, refer to the 10 MHz Reference (on the A15 RF assembly) troubleshooting procedure in Chapter 11.
3. Set the HP 8560E's **SPAN** to zero.
4. Reconnect W22.
5. With an oscilloscope probe, monitor A3J401 pin 20.
6. If TTL pulses are absent, the A2 controller assembly is faulty. Refer to Chapter 9. The presence of TTL pulses indicates a faulty A3 assembly.
7. Monitor A3J401 pin 23 (HBADC\_CLK0). If a 1 MHz TTL clock signal is present, HBADC\_CLK0 is working properly.
8. If HBKT\_PULSE or HBADC\_CLK0 is missing, disconnect A3W1 from A2J2.
9. Monitor A2U5 pin 3 for HBKT\_PULSE and A2U5 pin 7 for HBADC\_CLK0.
10. If HBADC\_CLK0 is absent, troubleshoot the A2 controller assembly.
11. HBKT\_PULSE is absent, refer to the information on troubleshooting the frequency counter in Chapter 9.
12. Reconnect A3W1 to A2J2.

## ADC Start/Stop Control

Refer to function block B of A3 Interface Assembly Schematic Diagram (sheet 2 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The ADC Start/Stop Control determines the start time of all ADC conversions. Multiplexer A3U509 chooses the source of the start signal. Both HSTART\_SRC and HBUCKET tell the ASM to start a conversion.

1. Press **PRESET** on the HP 8560E and set the following controls:

Span ..... 0 Hz  
Sweep time ..... 60 s  
Detector mode ..... SAMPLE

2. Check for a TTL high at A3U509 pin 2 and a TTL low at A3U509 pin 14.

3. Set the detector mode to NORMAL.

4. Check that A3U509 pins 2 and 14 are both TTL low.

5. Set the HP 8560E to the following settings:

Span ..... 1 MHz  
Detector mode ..... SAMPLE

6. Check for a TTL high at A3U509 pin 2 and a TTL low at A3U509 pin 14.

7. Press **CAL** and **REALIGN LO & IF**. During the realignment, A3U509 pin 2 should be TTL low and pin 14 should be TTL high until the 10 kHz and narrower resolution bandwidths are adjusted. If correct, the Start/Stop Control circuitry is being selected properly by the processor and U508 in the ADC Register block is working properly.

8. Press **PRESET** on the HP 8560E and set the controls as follows:

Span ..... 0 Hz  
Detector mode ..... SAMPLE  
Sweep time ..... 400 ms

9. Check that A3U509 pin 7 has positive 15  $\mu$ s pulses with a 667  $\mu$ s period (sweep time/600). Check that A3U509 pin 9 has positive 15  $\mu$ s pulses with a 667  $\mu$ s period (sweep time/600). The pulses should be present during the sweep but absent during retrace.

10. Set the detector mode to NORMAL.

11. Check that A3U509 pin 9 has pulses every 130  $\mu$ s and U509 pin 7 has pulses every 667  $\mu$ s (although pulse widths may be changing).

## ADC ASM

Refer to function block F of A3 Interface Assembly Schematic Diagram (Sheet 2 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

1. Press **PRESET** on the HP 8560E and set the controls as follows:  
Span ..... 0 Hz  
Sweep time ..... 60 s  
Detector mode ..... SAMPLE
2. Check that HSTART\_SRC (U504 pin 4) goes TTL high, causing HHOLD (U506 pin 16) to go high 15  $\mu$ s later.
3. Check that HSTART\_ADC (U506 pin 15) goes TTL high 19  $\mu$ s after HSTART\_SRC goes high.
4. HHOLD should stay TTL high for approximately 18  $\mu$ s, and HSTART\_ADC should stay high for approximately 31  $\mu$ s.
5. Check that LCMPLT (U504 pin 15) goes TTL low 12  $\mu$ s after HSTART\_ADC goes high (12 bits at 1  $\mu$ s per bit). LCMPLT indicates that the successive approximation state machine (SASM) has completed the ADC conversion.
6. Check that LDONE (U506 pin 19) goes TTL low approximately 2  $\mu$ s after LCMPLT goes low.

## ADC

Refer to function block A of A3 Interface Assembly Schematic Diagram (sheet 2 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The successive approximation state machine (SASM) consists of A3U527 and A3U528. Upon the occurrence of HSTART\_ADC, the SASM successively toggles bits from high to low starting with the most significant bit. The digital result is then converted to an analog current in DAC U518 and compared with the SAMPLED VIDEO. If the DAC current is too high, the output of U512 will be low, telling the SASM that the “guess” was high and that the bit just toggled should remain low. It then moves on to the next most significant bit until all 12 bits have been “guessed” at. Each “guess” takes 1  $\mu$ s (one cycle of HBADC\_CLK0), or 12  $\mu$ s to complete a conversion. When the conversion is completed, the SASM sets LCMPLT low. The bits are written to the data bus by buffers U514 and U516.

1. Set the HP 8560E controls as follows:

|                  |         |
|------------------|---------|
| Center frequency | 300 MHz |
| Span             | 0 Hz    |
| Sweep time       | 60 s    |
| Detector mode    | SAMPLE  |

2. Trigger an oscilloscope on HSTART\_ADC (U506 pin 15) and monitor the outputs of the SASM (U527 pins 18 and 19; U528 pins 14 thru 23). Each bit should start high and be switched low. It will either stay low or return to a high state 1  $\mu$ s later, depending on the comparison at U512.
3. If the outputs do not exhibit this bit pattern, and the ADC ASM checks are working properly, suspect A3U527, U528, or one of the latches (U514/516). If the output of comparator U512 does not toggle back and forth during a conversion, suspect either U512 or one of the clipping diodes (CR500/CR501).

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### Note

Because currents are being summed at U512 pins 2 and 3, voltage levels at these points are difficult to interpret.

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## Ramp Counter

Refer to function block D of A3 Interface Assembly Schematic Diagram (sheet 2 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The ramp counter is used for sweeps with widths greater than 2.0 MHz times N. The analog sweep ramp is compared to the digital ramp counter. When the analog sweep ramp exceeds the DAC output generated for that ramp counter setting, HRAMP\_COMP toggles high, indicating the end of a bucket. The ramp counter counts horizontal buckets. There are 601 buckets per sweep, so the ramp (bucket) counter counts from 0 to 600. The ramp counter is incremented by HRST\_PK\_ENA.

1. Press **PRESET** on the HP 8560E and set the controls as follows:

|               |        |
|---------------|--------|
| Span          | 5 MHz  |
| Detector mode | SAMPLE |

2. For spans greater than 2.0 MHz times N0, HODD (A3U525 pin 3) is a square wave with a period defined by  $(2 \times \text{sweep time}/600)$ . For example, for a 6 s sweep time, HODD has a period of 20 ms. The ramp (bucket) counter will be odd every other bucket.

## A3 Assembly's Control Circuits

A digital control problem will cause the following three steps to fail.

1. On the HP 8560E, press **AMPLITUDE**, **ATTEN MAN**, 7, 0, and **dB**.
2. A click should be heard after pressing dB in step 1, unless ATTEN was previously set to 70 dB.
3. Press 1, 0, and **dB**. Another click should be heard. If no clicks were heard, but the ATTEN value displayed on the CRT changed, the digital control signals are not operating properly.

## Analog Bus Drivers

Refer to function block N of A3 Interface Assembly Schematic Diagram (sheet 4 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

1. Press **PRESET** on the HP 8560E, and set the controls as follows:  
Span ..... 0 Hz  
Trigger ..... Single
2. Monitor A3U401 pin 3 (LRF\_STB) with an oscilloscope or logic probe. This is the strobe for the A15 RF Assembly.
3. Press **AUX CTRL** and **REAR PANEL** and check that pulses occur when toggling between **10 MHz INT** and **10 MHz EXT**.
4. Monitor U401 pin 5 (LFC\_STB) with an oscilloscope or logic probe. This is the strobe for the A14 frequency control assembly.
5. Press **AMPLITUDE** and check that pulses occur when toggling between **ATTEN** settings of 10 and 20 dB.
6. Monitor U401 pin 7 (LIF\_STB) with an oscilloscope or logic probe. This is the strobe for the A5 IF assembly.
7. Press **AMPLITUDE** and check that pulses occur when toggling between **REF LVL** settings of -10 dBm and -20 dBm.
8. Monitor U401 pin 9 (LLOG\_STB) with an oscilloscope or logic probe. This is the strobe for the log amplifier on the A4 assembly.
9. Press **AMPLITUDE** and check that pulses occur when toggling between **LINEAR** and **LOG dB/DIV**.
10. To check the Address and Data Lines, place a jumper from A3TP1 and A3TP2 to A3U406 pin 20 (+5 V).
11. Check that address lines A0 through A7 and data lines D0 through D7 are all TTL high.
12. If any address or data line is low, press **LINE** to turn spectrum analyzer off and disconnect the W2 control cable from A3J2. Press **LINE** to turn spectrum analyzer on. Ignore any error messages.

13. Check that address lines A0 through A7 and data lines D0 through D7 are all high. If all address and data lines are high, suspect a fault either in W2 or one of the other four assemblies which connect to W2.
14. If any address or data line is low, check the appropriate input of either U405 (data lines) or U406 (address lines).
15. If a data line input is stuck low, check the data bus buffer. If an address line input is stuck low, check A3W1 and the A2 controller assembly.
16. If the appropriate input is high or toggling between high and low, suspect a failure in either U405 (data lines) or U406 (address lines).
17. Remove jumpers.

## Analog Bus Timing

Refer to function block P of A3 Interface Assembly Schematic Diagram (sheet 4 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

Analog bus timing (ABT) generates the strobes for the A4, A5, A14, and A15 assemblies. The A14 frequency control assembly also requires a qualifier for its strobe, LVFC\_ENABLE. A3U400 and A3U414 provide a 2  $\mu$ s delay between the time HANA\_BUS goes high and the enable line to demultiplexer A3U407 goes low.

1. Press **PRESET** on the HP 8560E and set the controls as follows:
 

|                  |               |
|------------------|---------------|
| Center frequency | ..... 300 MHz |
| Span             | ..... 100 MHz |
2. Check that A3U407 pin 1 goes low approximately 2  $\mu$ s after HANA\_BUS (A3U400 pin 3) goes high.
3. If HANA\_BUS is absent, check for pulses on ABT A3U505 pin 2 and IA10 (A3U505 pin 5).
4. If A3U407 pin 1 is not delayed 2  $\mu$ s from HANA\_BUS, check for the presence of the 1 MHz HBADC\_CLK0.
5. If A3U407 pin 1 is not delayed 2  $\mu$ s from HANA\_BUS and HBADC\_CLK0 is correct, suspect a fault in either A3U414 or A3U400.
6. Press **PRESET** and set the controls as follows:
 

|         |              |
|---------|--------------|
| Span    | ..... 0 Hz   |
| Trigger | ..... SINGLE |
7. Monitor A3U401 pin 3 (LR\_STB) with an oscilloscope or logic probe. This is the strobe for the A15 RF assembly.
8. Press **AUX CTRL** and **REAR PANEL** and check that pulses occur when toggling between **10 MHz INT** and **10 MHz EXT**.
9. Monitor A3U401 pin 5 (LF\_STB) with an oscilloscope or logic probe. This is the strobe for the A14 frequency control assembly.
10. Press **AMPLITUDE** and check that pulses occur when toggling between **ATTEN** settings of 10 and 20 dB.

11. Monitor A3U401 pin 7 (LI\_STB) with an oscilloscope or logic probe. This is the strobe for the A5 IF assembly.
12. Press **AMPLITUDE** and check that pulses occur when toggling between **REF LVL** settings of -10 dBm and -20 dBm.
13. Monitor A3U401 pin 9 (LV\_STB) with an oscilloscope or logic probe. This is the strobe for the A4 log amplifier/cal oscillator assembly.
14. Press **AMPLITUDE** and check that pulses occur when toggling between **LINEAR** and **LOG DB/DIV**.

### Interface Strobe Select

Refer to function block K of A3 Interface Assembly Schematic Diagram (sheet 3 of 6) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

Interface strobe select generates the various strobes used by circuits on the A3 Interface Assembly. Table 7-10 and Table 7-11 are the truth tables for demultiplexers A3U410 and A3U500.

**Table 7-10. Demultiplexer A3U410 Truth Table**

| Selected Output Line | IA1 | IA2 | IA3 |
|----------------------|-----|-----|-----|
| Pin 15, LSCAN_KBD    | L   | L   | L   |
| Pin 14, LDACU1       | H   | L   | L   |
| Pin 13, LDAC1        | L   | H   | L   |
| Pin 12, LDAC2        | H   | H   | L   |
| Pin 11, LDAC3        | L   | L   | H   |
| Pin 10               | H   | L   | H   |
| Pin 9, LTIMER        | L   | H   | H   |
| Pin 7, LADC_REG1     | H   | H   | H   |

**Table 7-11. Demultiplexer A3U500 Truth Table**

| Selected Output Line | IA0 | IA1 | IA2 |
|----------------------|-----|-----|-----|
| Pin 15, LSENSE_KBD   | L   | L   | L   |
| Pin 14, LINT_PRIOR   | H   | L   | L   |
| Pin 13, LADC_DATA1   | L   | H   | L   |
| Pin 12, LDAC_DATA0   | H   | H   | L   |
| Pin 11, HCNTR_LD0    | L   | L   | H   |
| Pin 10, HCNTR_LD1    | H   | L   | H   |
| Pin 9, LRPGRD        | L   | H   | H   |
| Pin 7, LADC_REG0     | H   | H   | H   |

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## A16 Assembly's Fast ADC Circuits (Option 007)

The fast ADC consists of video signal scaling and limiting amplifiers, an 8-bit flash ADC, peak/pit detection of the digitized video signal, a 32 K-byte RAM, and the fast ADC control circuitry.

### Video Input Scaling Amplifiers and Limiter

Refer to function block L of the A16 fast ADC assembly schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The video input scaling amplifiers help provide scaling (10 dB/div, 5 dB/div, 2 dB/div, or 1 dB/div) and buffer the flash video output. When the GAINX2 control line is low, switch U44D is open and switch

U44C is closed. Thus, the scaled video at TP26 virtually follows the video input (0 - 1 V). When the GAINX2 control line is high, switch U44C is open and switch U44D is closed. Amplifier U43 then provides a gain of  $2(V_{in}) - 1$  V. Voltage clamp CR4 prevents the scaled video input to amplifier U45 from going more negative than -0.35 V or more positive than +1.25 V.

---

|             |                                                                                                                                                                                                                       |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note</b> | When measuring voltages or waveforms on the A16 fast ADC assembly, connect the ground (or common) lead to the ground-plane trace on the A16 assembly. This digital ground plane is totally isolated from the chassis. |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

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1. Press **PRESET** on the HP 8560E Option 007 and set the controls as follows:

|                  |                 |
|------------------|-----------------|
| Center frequency | ..... 300 MHz   |
| Span             | ..... 0 Hz      |
| Reference level  | ..... -10 dBm   |
| Log/division     | ..... 10 dB/div |
| Sweep time       | ..... 20 ms     |
2. Connect the CAL OUTPUT to the INPUT 50 $\Omega$  connector.
3. Adjust the HP 8560E Option 007 reference level to place the signal at the top graticule line on the CRT display.
4. Measure the dc level at TP25. If the voltage measured is not  $+1.0 \pm 0.15$  V, troubleshoot the A3 interface assembly.
5. Measure the dc level at TP26. The level should be approximately the same as the level measured at TP25. If not, suspect switch U44.
6. Set the HP 8560E Option 007 scale to 5dB per division.
7. Adjust the HP 8560E Option 007 reference level to place the signal at the top graticule line on the CRT display.
8. Measure the dc level at TP25 and TP26. The level should be  $+1.0 \pm 0.25$  V. If the level measured at TP26 differs from the level measured at TP25 by more than 0.25 volts, troubleshoot U43 and associated circuitry.
9. Disconnect the CAL OUTPUT signal from the INPUT 50 $\Omega$  connector.

10. The level at TP26 should drop to  $-0.35$  Vdc. If the level is less (more negative) than  $-0.35$  Vdc, replace voltage clamp CR4.
11. Measure the dc level of the flash video at TP27. The level should be near 0 Vdc with the signal at the bottom graticule line (no input to the spectrum analyzer).
12. Connect the CAL OUTPUT to the INPUT  $50\Omega$  connector.
13. Measure the dc level of the flash video at TP27. The level should be near  $+1.7$  Vdc.

## 8-Bit Flash ADC

Refer to function block I of the A16 fast ADC assembly schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The flash ADC (U35) converts the analog video signal into 8-bit digital values at a fixed rate of 12 megasamples per second.

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**Note** When measuring voltages or waveforms on the A16 fast ADC assembly, connect the ground (or common) lead to the ground-plane trace on the A16 assembly. This digital ground plane is totally isolated from the chassis.

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1. Press **PRESET** on the HP 8560E Option 007 and set the controls as follows:
 

|                  |       |            |
|------------------|-------|------------|
| Center frequency | ..... | 300 MHz    |
| Span             | ..... | 0 Hz       |
| Reference level  | ..... | $-20$ dBm  |
| Log/division     | ..... | $5$ dB/div |
| Sweep time       | ..... | 20 ms      |
2. Connect the CAL OUTPUT to the INPUT  $50\Omega$  connector.
3. Pins 4 through 10 (ADC7-ADC1) and pin 21 (ADC0) of U35 should all be high (logic 1), corresponding to an ADC digital count of 255 for the analog input of  $+2$  volts or greater.
4. Disconnect the CAL OUTPUT signal from the INPUT  $50\Omega$  connector.
5. Pins 4 through 10 (ADC7-ADC1) and pin 21 (ADC0) of U35 should all be low (logic 0), corresponding to an ADC digital count of zero for the analog input of 0 volts or less.

## Peak/Pit Detection

Refer to function block J of the A16 fast ADC assembly schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

Peak detection or pit (negative peak) detection can be enabled whenever the sample rate is less than 12 MHz (sweep times greater than  $50\ \mu\text{s}$ ). Peak detection uses the maximum value of all the samples taken within each bucket (between adjacent display points). Pit detection uses the minimum value of all the samples taken within each bucket. And sample detection uses the last sample of all the samples taken within each bucket.

The different detection modes are implemented by selectively clocking latch U30, depending on the state of LP/Q which is generated in PAL U1 (block A). When LP/Q is low, U30 is clocked by WCLK. When LP/Q is high, U30 is not clocked. LP/Q is a function of the 12M\_SEL, SCLK-1, LSAMPLE, LPEAK, P\_LO, and P\_HI signals. See Table 7-12.

If the sample rate is 12 MHz, 12M\_SEL is high, which forces LP/Q low so that every sample is clocked into latch U30 and latched into RAM U32 (block K). If the sample rate is less than 12 MHz and the detection mode is peak or pit, the SCLK-1, LPEAK, P\_LO, and P\_HI signals control the LP/Q signal. In these detection modes, latch U30 stores the peak or pit value of the samples taken for each bucket. The 8-bit digital magnitude comparator, U31, compares the input byte (P) with the output byte (Q) from latch U30. When P is greater than Q, P\_LO is low (0) and P\_HI is high (1). When P is less than Q, P\_LO is high (1) and P\_HI is low (0). When P is equal to Q, P\_LO and P\_HI are both low (0). See Table 7-12.

**Table 7-12. LP/Q Truth Table**

| Mode                           | LP/Q | 12M_SEL | SCLK-1 | LSAMPLE | LPEAK | P_LO | P_HI |
|--------------------------------|------|---------|--------|---------|-------|------|------|
| 12MHz                          | L    | H       | X      | X       | X     | X    | X    |
| SAMPLE                         | L    | X       | X      | L       | X     | X    | X    |
| POS<br>PEAK                    | L    | L       | L      | H       | L     | L    | H    |
|                                | H    | L       | L      | H       | L     | H    | L    |
|                                | H    | L       | L      | H       | L     | L    | L    |
| NEG<br>PEAK<br>(Pit)           | H    | L       | L      | H       | H     | L    | H    |
|                                | L    | L       | L      | X       | H     | H    | L    |
|                                | H    | L       | L      | H       | H     | L    | L    |
| Clocking<br>Peak/Pit<br>Sample | L    | L       | H      | H       | X     | X    | X    |

### 32 K-Byte Static RAM

Refer to function block K of the A16 fast ADC assembly schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The static RAM stores the flash ADC samples that are taken when the fast ADC circuitry is in the “write” mode. When not in the “write” mode, the static RAM is read by the CPU on the A2 controller assembly to retrieve the fast ADC data.

The 8-bit Q bus connects the outputs of latch U30 to the data port of static RAM U32.

## A16 Assembly's Fast ADC Control Circuits (Option 007)

The fast ADC control circuits consist of the CPU interface and control registers, the reference clock, a clock and sample rate generator, a trigger circuit, a 16-bit post-trigger counter, a 15-bit circular address counter, a video trigger comparator, and the reference and power supply circuits.

### CPU Interface and Control Registers

Refer to function block A of the A16 fast ADC assembly schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The A16 assembly's digital interface to the A2 controller assembly consists of an 8-bit bi-directional data bus, one address line, a most-significant byte strobe, and a least-significant byte strobe.

The A16 fast ADC assembly can be accessed by firmware (on the A2 controller assembly) at two logical addresses. When the address line (ADDR3) is low, the primary address is selected. When the ADDR3 is high, the secondary address is selected. The data transfers between the A16 fast ADC assembly and the A2 controller assembly are clocked by the two strobe lines, MSB\_STRB and LSB\_STRB. 16-bit word transfers occur as two sequential byte transfers; the most-significant byte first, followed by the least-significant byte.

The primary address (ADDR3 low) contains the 16-bit control word written by the firmware on the A2 controller assembly. The secondary address (ADDR3 high) supports both 8-bit byte and 16-bit word reads and writes. There is no read/write line on the A16 fast ADC assembly to control the direction of data transfer. The fast ADC is preconfigured to read or write by setting the appropriate bits in the 16-bit control word. Refer to Table 7-13. If the control word is not correct, it may result in a bus conflict.

**Table 7-13. Control Word at Primary Address (U3 and U4)**

| Bit   | Mnemonic | State | Description                                                                                                                       |
|-------|----------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| Bit 0 | WRITE    |       | Allows samples to be written to FADC memory.                                                                                      |
|       |          | 1     | All on-board clocks running and samples being written to FADC memory. (FADC memory cannot be read by A2 controller in this mode.) |
|       |          | 0     | All on-board clocks turned off and no samples being written to FADC memory. (FADC memory can be read by A2 controller.)           |
| Bit 1 | ARM      |       | Arms the FADC assembly for a trigger.                                                                                             |
|       |          | 1     | FADC assembly armed to accept trigger from HSWP line or video trigger.                                                            |
|       |          | 0     | FADC assembly cannot be triggered.                                                                                                |

**Table 7-13. Control Word at Primary Address (U3 and U4) (continued)**

| Bit   | Mnemonic  | State | Description                                                                                                                                                     |
|-------|-----------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit 2 | GAINX2    |       | Turns on X2 log expand amplifier.                                                                                                                               |
|       |           | 1     | A16U43 turned on. (5 dB/div or 1 dB/div scale)                                                                                                                  |
|       |           | 0     | A16U43 turned off. (10 dB/div, 2 dB/div, or linear scale)                                                                                                       |
| Bit 3 | VTRIG_POL |       | Controls digital video trigger polarity.                                                                                                                        |
|       |           | 1     | Negative-edge video trigger                                                                                                                                     |
|       |           | 0     | Positive-edge video trigger                                                                                                                                     |
| Bit 4 | LSAMPLE   |       | Enables sample detection mode.                                                                                                                                  |
|       |           | 1     | Sample detection mode disabled.                                                                                                                                 |
|       |           | 0     | Sample detection mode enabled.                                                                                                                                  |
| Bit 5 | LADCEN    |       | Enables FADC memory for "writes". (Toggled in conjunction with bit 0.)                                                                                          |
|       |           | 1     | Disables FADC memory for "writes".                                                                                                                              |
|       |           | 0     | Enables FADC memory for "writes".                                                                                                                               |
| Bit 6 | LLOADADDR |       | Enables load address counter.                                                                                                                                   |
|       |           | 1     | "Writes" to the address counter disabled.                                                                                                                       |
|       |           | 0     | "Writes" to the address counter enabled.                                                                                                                        |
| Bit 7 | LLOADPOST |       | Enables load post-trigger counter.                                                                                                                              |
|       |           | 1     | "Writes" to the post-trigger counter disabled.                                                                                                                  |
|       |           | 0     | "Writes" to the post-trigger counter enabled.                                                                                                                   |
| Bit 8 | LVTRIG_EN |       | Enables digital video trigger on A16.                                                                                                                           |
|       |           | 1     | Digital video trigger disabled.                                                                                                                                 |
|       |           | 0     | Digital video trigger enabled.                                                                                                                                  |
| Bit 9 | LREADCLK  |       | Clocks counters during "read" mode. Used to load post-trigger counter or address counter. Also used to post-increment address counter following memory "reads". |
|       |           | 1     | Read clock disabled.                                                                                                                                            |
|       |           | 0     | Read clock enabled.                                                                                                                                             |

**Table 7-13. Control Word at Primary Address (U3 and U4) (continued)**

| Bit    | Mnemonic   | State | Description                                                                 |
|--------|------------|-------|-----------------------------------------------------------------------------|
| Bit 10 | LREADMEM   |       | Enables read FADC memory.                                                   |
|        |            | 1     | Read FADC memory disabled.                                                  |
|        |            | 0     | Read FADC memory enabled.                                                   |
| Bit 11 | LREADADDR  |       | Enables read trigger address latch.                                         |
|        |            | 1     | “Reads” from trigger address latch disabled.                                |
|        |            | 0     | “Reads” from trigger address latch enabled.                                 |
| Bit 12 | LRATELATCH |       | Enables load sample rate latch.                                             |
|        |            | 1     | “Writes” to the sample rate latch are disabled.                             |
|        |            | 0     | “Writes” to the sample rate latch are enabled.                              |
| Bit 13 | LRLSHSWP   |       | Releases HSWP strobe.                                                       |
|        |            | 1     | Release HSWP strobe disabled.                                               |
|        |            | 0     | Release HSWP strobe enabled.                                                |
| Bit 14 | LLOADTRIG  |       | Enables load video trigger level.                                           |
|        |            | 1     | Load digital video trigger level disabled.                                  |
|        |            | 0     | Load digital video trigger level enabled.                                   |
| Bit 15 | LPEAK      |       | Peak/pit detection mode control.                                            |
|        |            | 1     | Enables pit (negative-peak) detection mode if LSAMPLE (Bit 4) is also high. |
|        |            | 0     | Enables peak detection mode if LSAMPLE (Bit 4) is high.                     |

## Reference Clock

Refer to function block B of the A16 fast ADC assembly schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The reference clock circuitry takes the 8 MHz CMOS square wave clock from the A2 controller assembly (via W59, coax 839) and triples the frequency to 24 MHz. Inverters U5A and U5B provide the proper match for the 8 MHz clock input, and also the desired drive level into the 24 MHz bandpass filter. The 24 MHz bandpass filter consists of R5, C8, L1, C9, C10, L2, C11, L3, C12, L4, C13, C14, and R6. Inverters U6A and U6B provide amplification of the 24 MHz clock to produce CMOS levels, and also buffer the 24 MHz clock output.

## Clock and Sample Rate Generator

Refer to function block C of the A16 fast ADC assembly schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The clock and sample rate generator takes the 24 MHz reference clock signal and generates all of the various clock signals used on the A16 fast ADC assembly. The sample rate generator consists of CMOS latch U15, CMOS counters U14 and U16, and CMOS flip-flops U7B and U9A. The sample rate generator only controls the rate at which the static RAM address counter (15-bit circular address counter) and the 16-bit post-trigger counter are clocked (ACLK and PCLK respectively). The sample rate generator also controls the number of flash ADC samples taken per bucket. The range of the sample rate is 1 sample per bucket (12 MHz rate) to 256 samples per bucket (less than 12 MHz rate). SCLK-1 is an input to PAL U1 (block A) and affects the LP/Q signal to ensure that the first sample of a bucket is always clocked into latch U30 (block J) and written into static RAM U32 (block K) when the detection mode is peak or pit and the sample rate is less than 12 MHz. Refer to Table 7-12, LP/Q Truth Table in this chapter.

## Trigger

Refer to function block D of the A16 fast ADC assembly schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

When the A16 fast ADC is triggered, the current static RAM address is latched into trigger address latches U27 and U28 (block G), and the

post-trigger counter (U19, U20, U21, U22, and U47) begins counting.

Samples continue to be written to consecutive addresses in RAM U32 until the post-trigger counter reaches its terminal count. The CPU on the A2 controller assembly monitors the HSWP line and starts a software timer when HSWP goes high after being triggered. The software timer is set to slightly longer than the post-trigger counter will be counting, so at the end of the "time-out", the post-trigger counter has already reached its terminal count. At the end of this "time-out", the CPU on the A2 controller assembly takes the fast ADC out of "write" mode and reads latches U27 and U28 to determine the static RAM address of the sample that was taken when the trigger occurred. The CPU then writes the trigger address (read at U27/U28) to the fast ADC static RAM address counter (15-bit circular address counter). If pre-trigger or post-trigger (delay) is being used, the CPU adds or subtracts appropriately and writes the "adjusted" trigger address to the static RAM counter. The CPU then begins reading the fast ADC data, starting from the trigger (or offset trigger) address.

The trigger circuitry is enabled by the ARM signal (bit 1 of the fast ADC control word). Once a trigger occurs, the fast ADC cannot be triggered again until the ARM line goes low (disarmed), then high again (armed).

The fast ADC is triggered by the HSWP line in **FREE RUN**, **LINE**, and **EXTERNAL** trigger modes. When **VIDEO** trigger is being used, a synchronous digital video trigger signal, VCLK, is generated by PAL U1 (block A) and U17A (block D).

## 16-Bit Post-Trigger Counter

Refer to function block E of the A16 fast ADC assembly schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The 16-bit post-trigger counter controls the number of static RAM memory locations that will be written after the trigger occurs. This counter consists of U19, U20, U21, U22, and U47. The counter is loaded from the CPU on the A2 controller assembly when the A16 fast ADC assembly is in “read” mode. The CPU loads the counter by first setting the LLOADPOST (bit 7 of the fast ADC control word) and the LREADCLK (bit 9 of the fast ADC control word) to their low state. The CPU then writes the 16-bit word to the fast ADC secondary address. The rising edge of PCLK then latches the 16-bit data into the post-trigger counter.

The post-trigger counter begins counting upward in “write” mode on the first rising edge of PCLK after the LCOUNT signal from the trigger circuit goes low. The frequency of PCLK is the programmed sample rate. When the post-trigger counter reaches its terminal count, the LSTOP signal goes low and disables the static RAM address counter from further counting. LSTOP also forces LCOUNT high in NAND gate U11D, which disables the post-trigger counter.

## 15-Bit (32 K) Circular Address Counter

Refer to function block G of the A16 fast ADC assembly schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

This 15-bit programmable circular counter provides the address lines of the static RAM (U32). The counter consists of U23, U24, U25, and U26. It counts upward from 0 to 32767 and then back to 0 in a circular fashion. When a trigger occurs, latches U27 and U28 latch the current static RAM address so that the CPU on the A2 controller assembly can later read the latches and determine the static RAM address of the sample that was taken when the trigger occurred.

The CPU loads the address counter during “read” mode by first setting LLOADADDR (bit 6 of the fast ADC control word) and LREADCLK (bit 9 of the fast ADC control word) to their low state. The CPU then writes the 16-bit load value to the CPU secondary address. The rising edge of ACLK then latches the 16-bit data into the address counter.

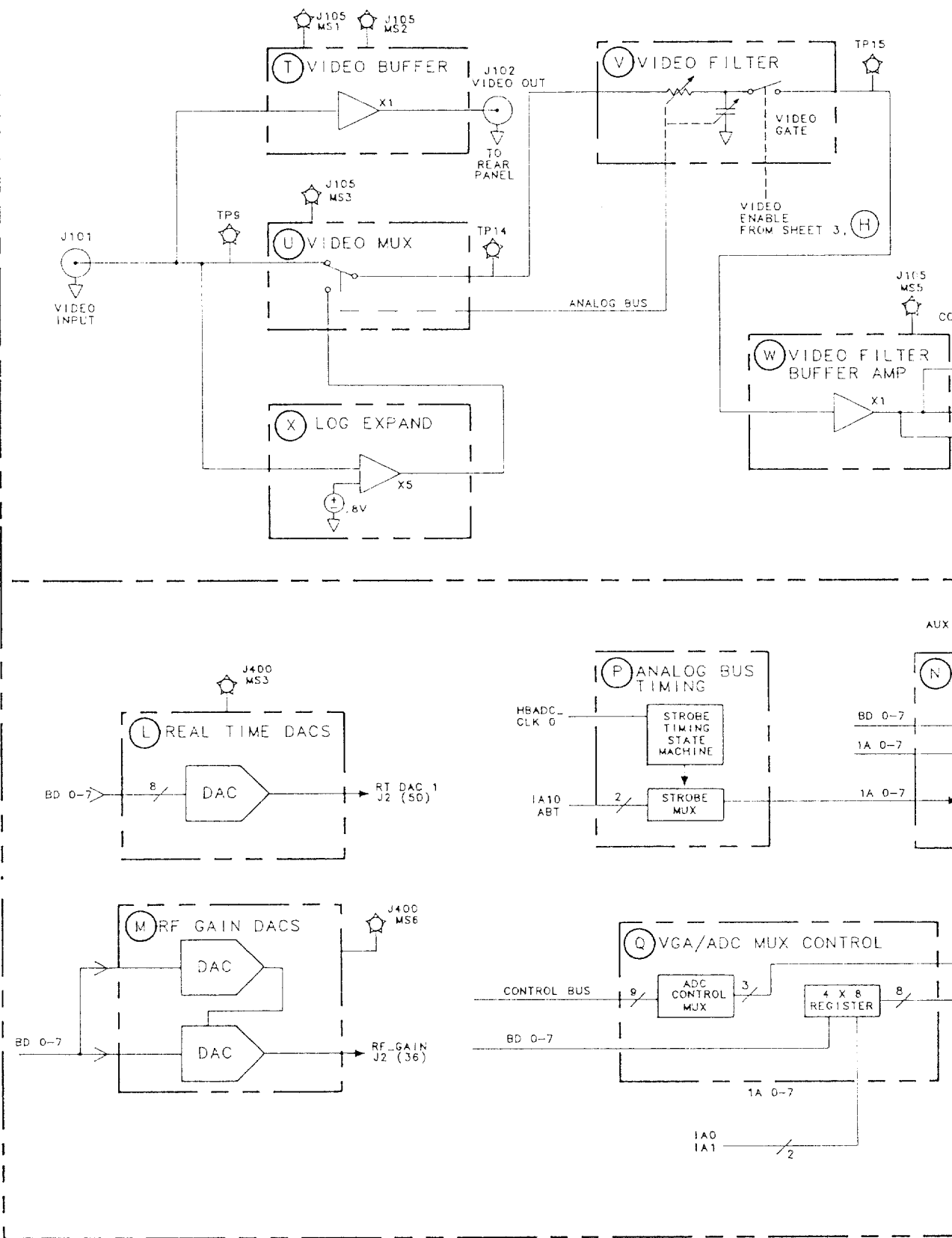
After the address counter is loaded by the CPU during “read” mode, the static RAM is read by the CPU. The RAM is read by first setting LREADMEM (bit 10 of the fast ADC control word) and LREADCLK (bit 9 of the fast ADC control word) to their low state. Since the LREADCLK control bit is low, a negative-going pulse on the ACLK line will occur on every static RAM “read” by the CPU. This causes the address counter to increment at the end of each static RAM “read” so that the address counter automatically post-increments to the next address of RAM U32. In order for this address post-increment to occur, the LSTOP count enable signal from the post-trigger counter must be high. LSTOP goes low when the post-trigger counter reaches its terminal count in the “write” mode to stop the address counter from counting. When the fast ADC assembly is changed from “write” mode to “read” mode, LSTOP will be low. So the CPU on the A2 controller board must always first program the post-trigger counter to a value other than the terminal count (65535) to force LSTOP high.

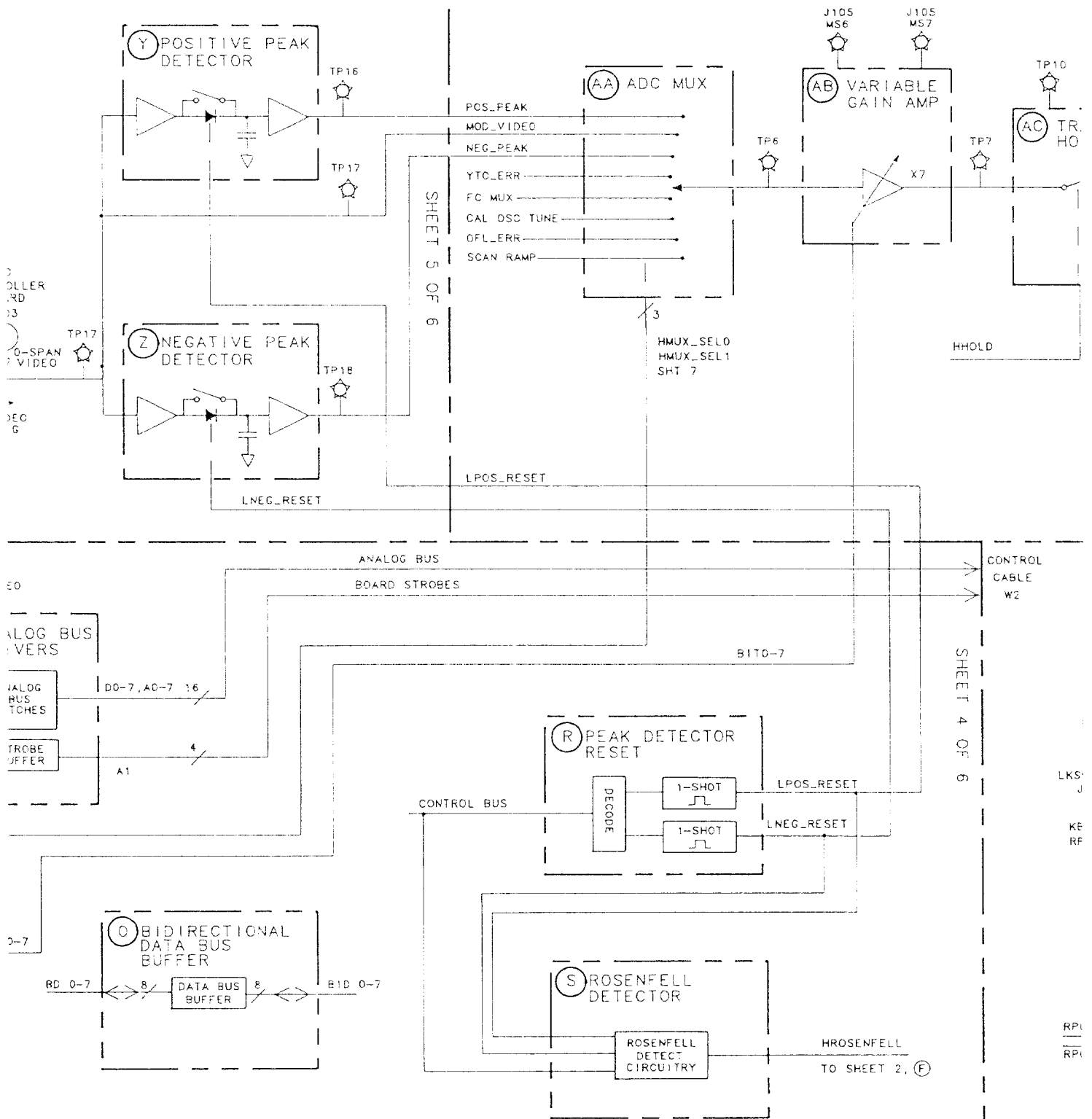
## Video Trigger Comparator

Refer to function block M of the A16 fast ADC assembly schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

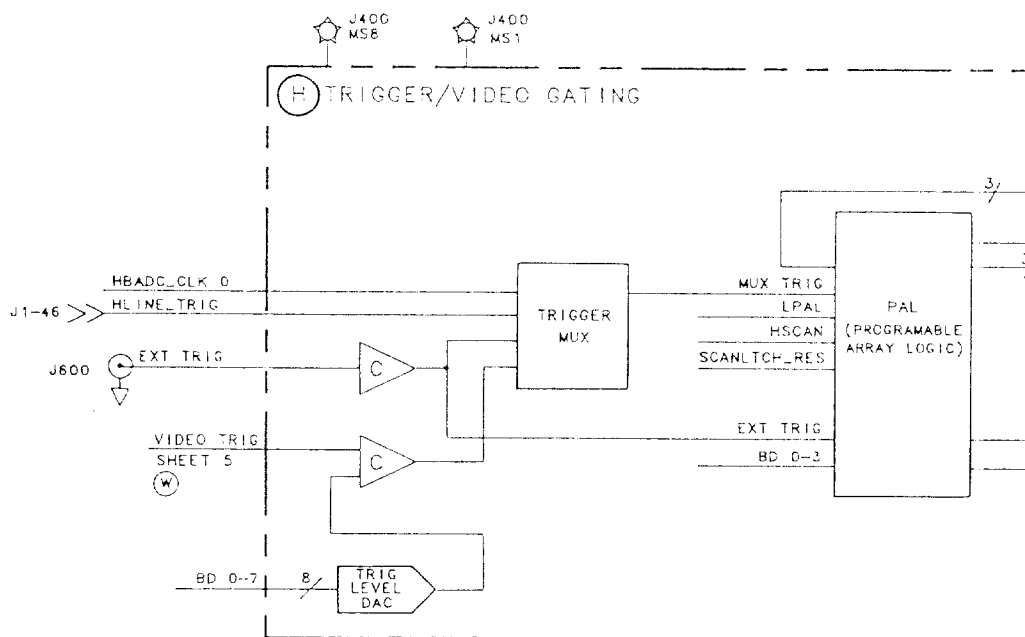
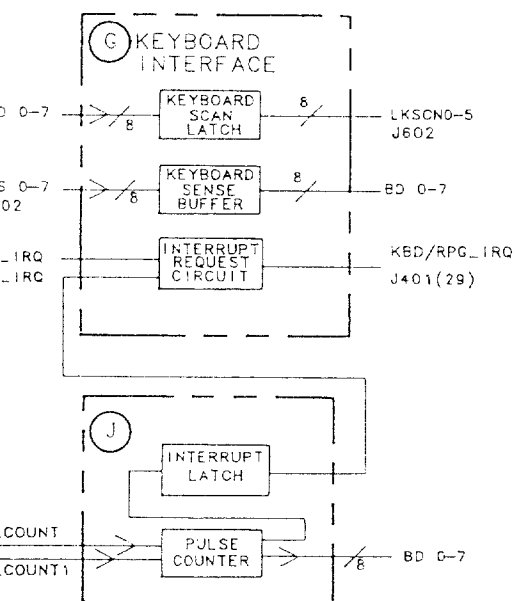
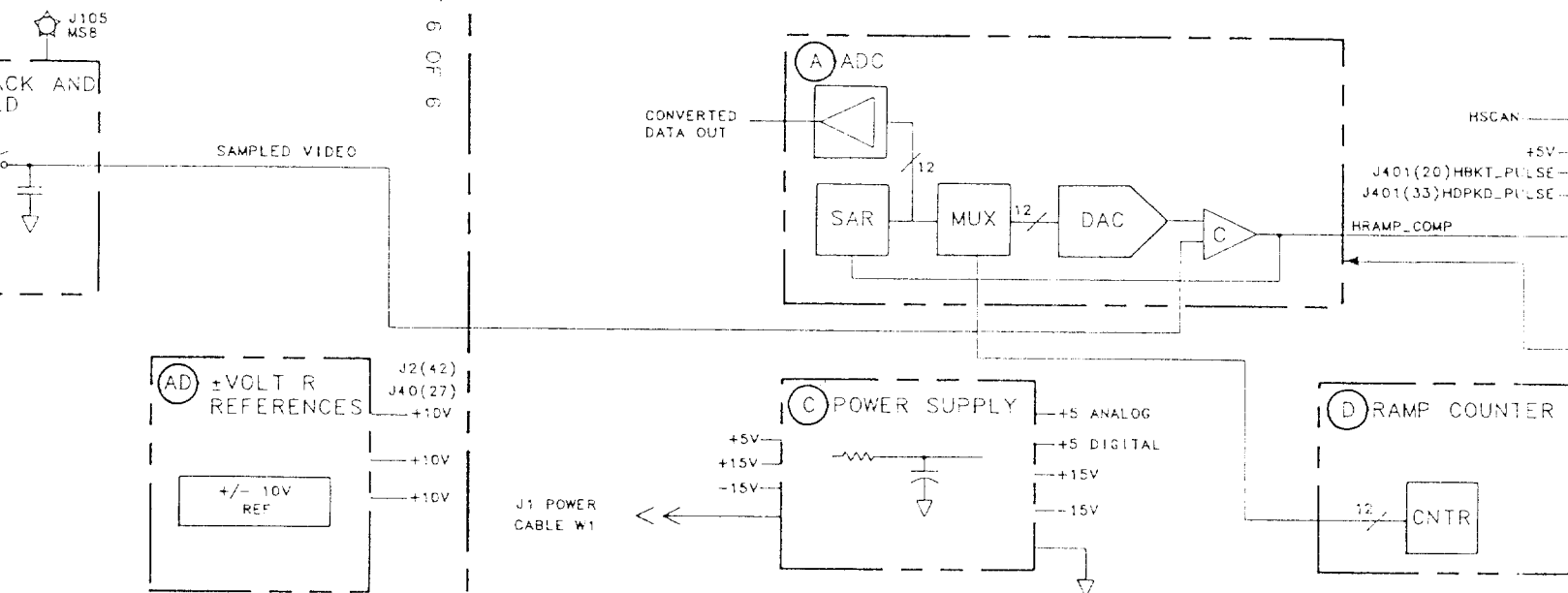
This 8-bit digital magnitude comparator, U34, compares the digitized samples from the flash ADC (latch U29 output) to the programmed video trigger level. The video trigger level value on IOB2 through IOB7 is latched into the P input (top portion of U34) by the firmware on the A2 controller assembly when the fast ADC is in "read" mode. When the sample on the Q input is higher than the video trigger level on the P input, V\_HI output is high, and V\_LO output is low. When the Q input is lower than the P input, V\_HI output is low and V\_LO output is high. And when P is equal to Q, both V\_HI and V\_LO are low. These two signals (V\_HI and V\_LO) go to PAL U1 (block A) and are used to clock the video trigger generator (block D).

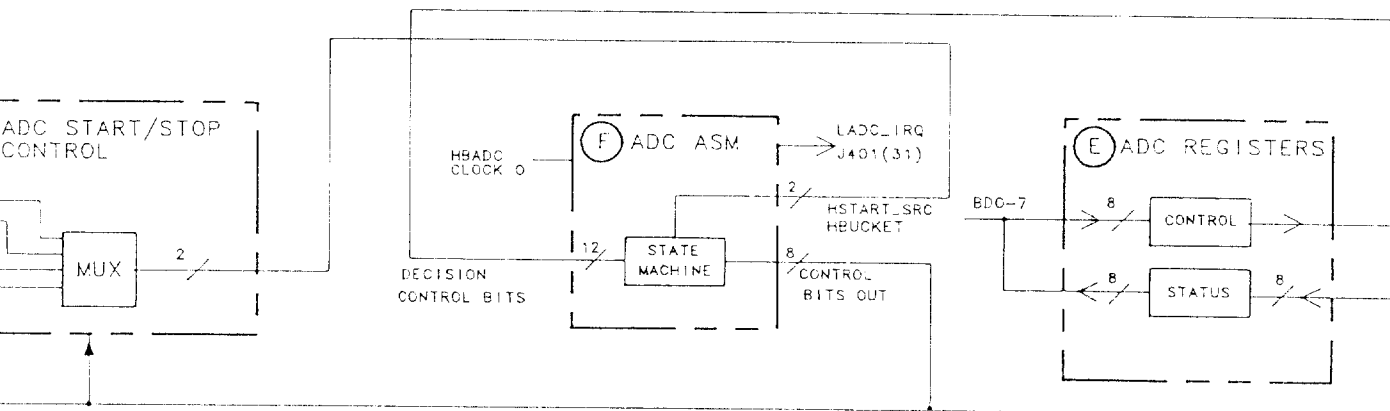
## A3 INTERFACE ASSEMBLY



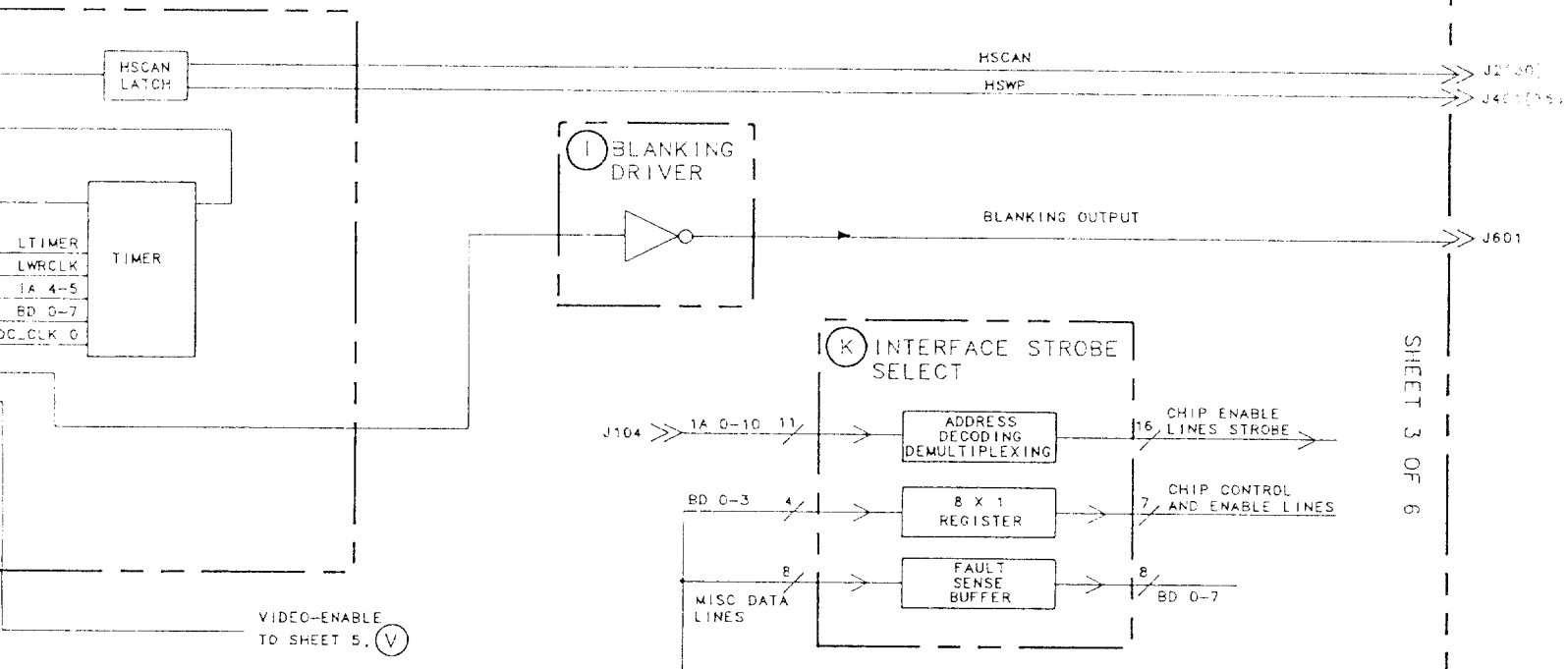


SHEET 6 OF 6



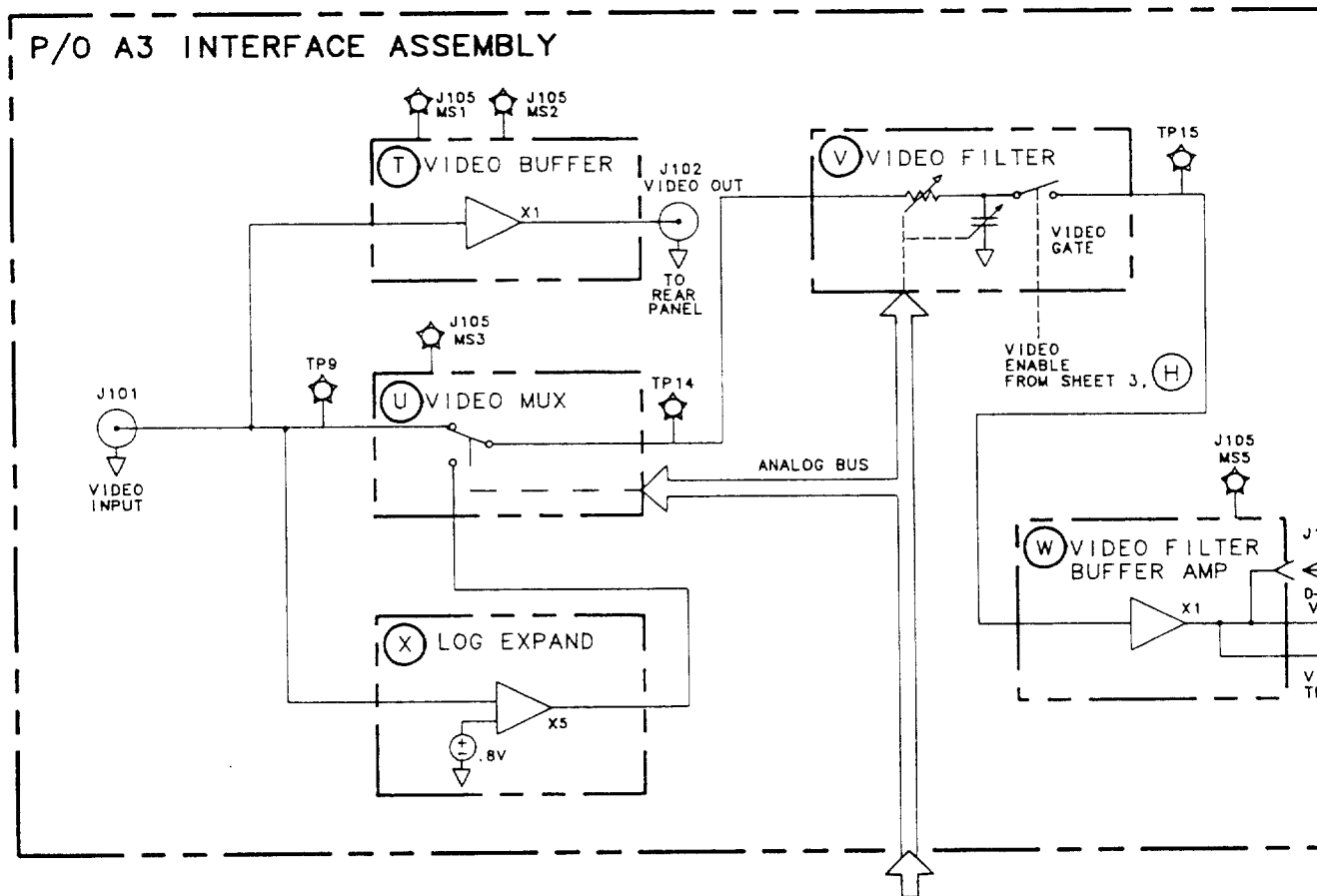


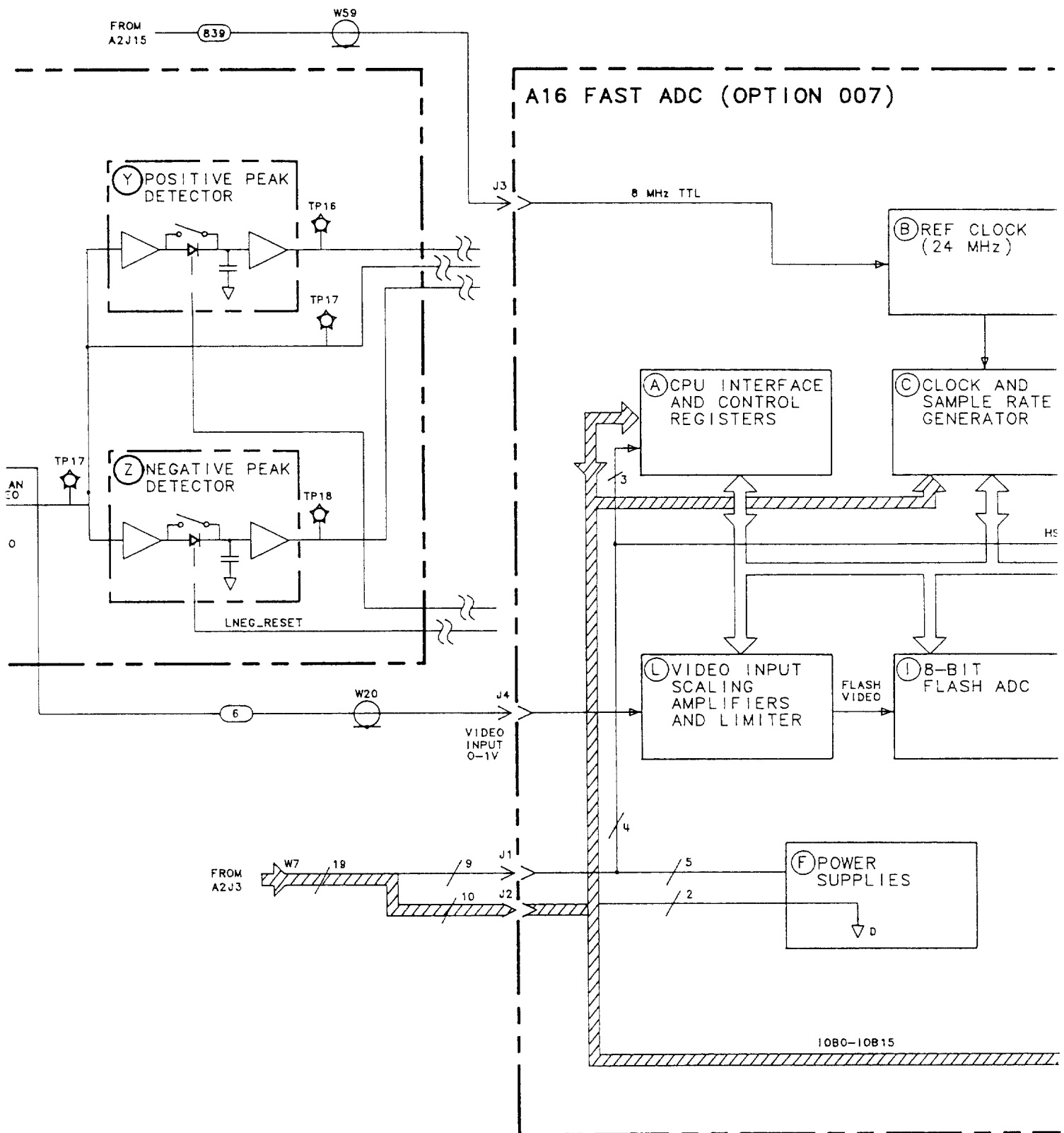
SHEET 2 OF 6



SHEET 3 OF 6

FIGURE 7-2. A3 INTERFACE ASSEMBLY BLOCK DIAGRAM

FAST ADC (OPTION 007)  
BLOCK DIAGRAM



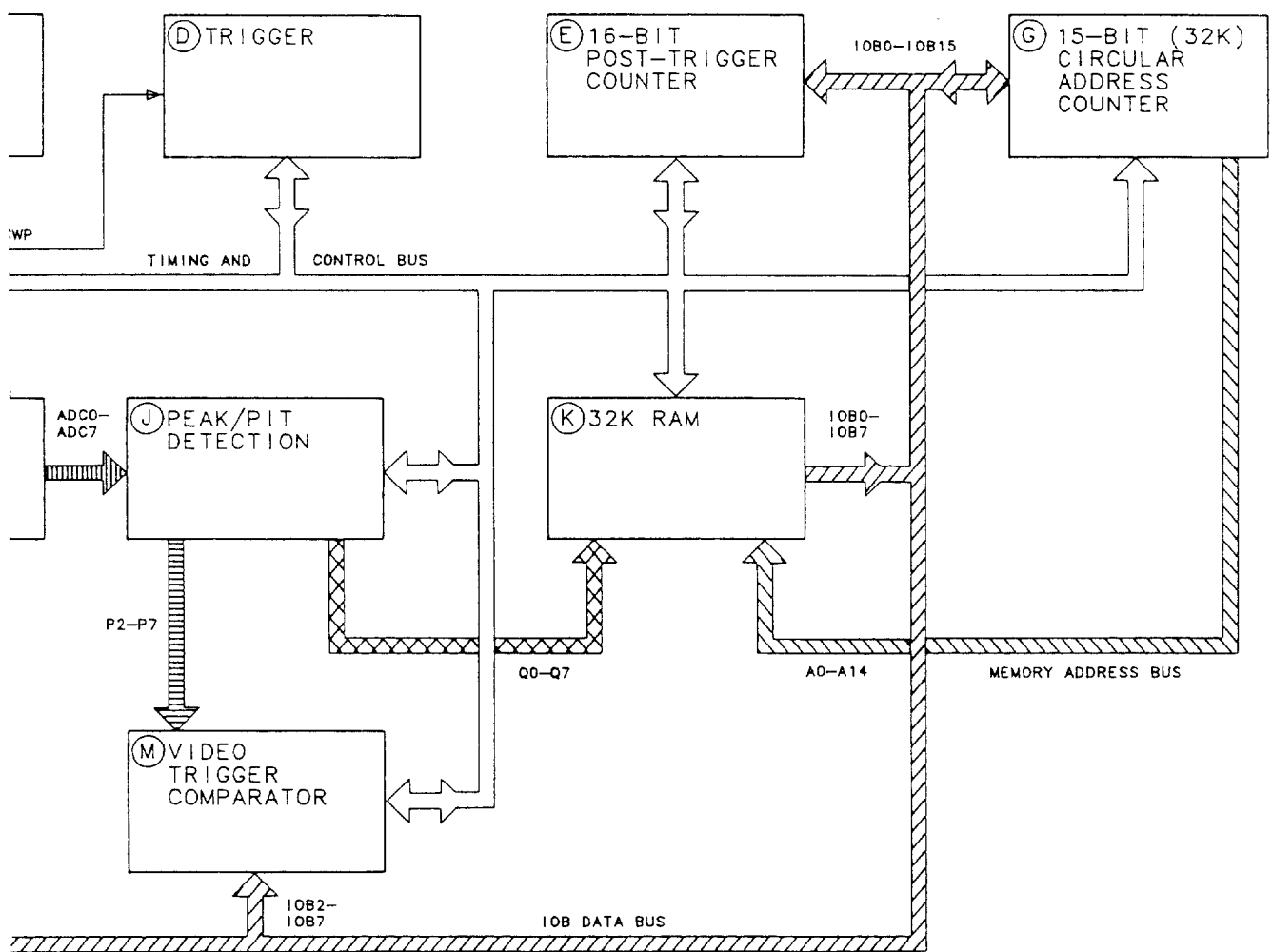


FIGURE 7-3. FAST ADC (OPTION 007) BLOCK DIAGRAM

## IF Section

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The IF Section contains the A4 Log Amplifier/Cal Oscillator and A5 IF assemblies.

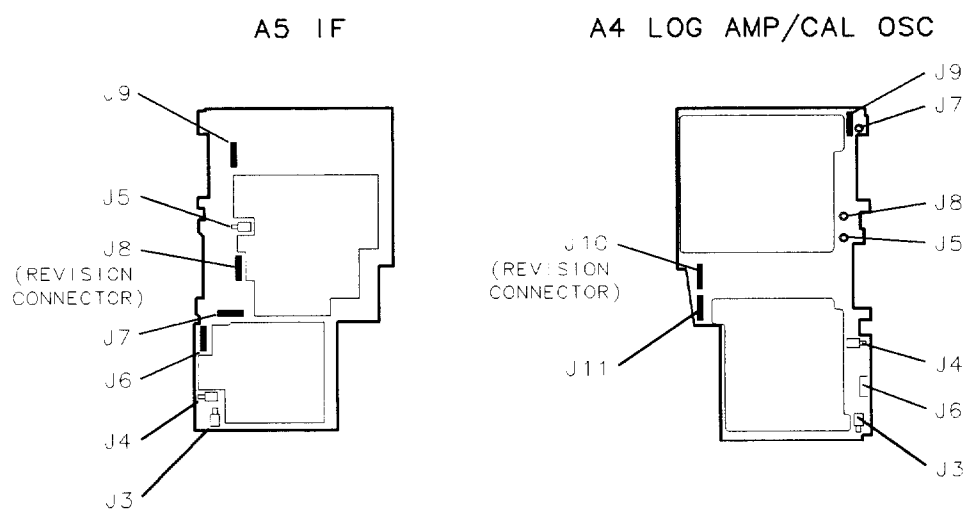
- Troubleshooting Using the TAM
  - Troubleshooting the Log Amplifier with the TAM
  - Troubleshooting A5 with the TAM
  - Troubleshooting the Cal Oscillator with the TAM
- Automatic IF Adjustment
  - Parameters Adjusted
  - Requirements
- Performance Test Failures
  - IF Gain Uncertainty Performance Test
  - Scale Fidelity Performance Test
  - Resolution Bandwidths Performance Tests
- Log Amplifier Assembly (P/O A4)
  - Log Amplifier
  - Linear Amplifiers
  - Video Offset
  - Video Output
  - Frequency Counter Prescaler/Conditioner
  - AM/FM Demodulator
  - 4.8 kHz IF Filters
  - 10.7 MHz IF Filters
  - 4.8 kHz and 10.7 MHz IF Filters
  - 10.6952 MHz VCXO
  - Input Switch
  - LO Switch
  - Synchronous Detector
    - Limiter
    - Isolation Amplifier
    - Detector/Mixer
  - Log Offset/Gain Compensation
    - Log Offset Compensation
    - Log Gain Compensation
  - Video MUX
- A5 IF Assembly
  - IF Signature
    - Common IF Signature Problems
    - 1 MHz Resolution Bandwidth Problems
    - 30 kHz Resolution Bandwidth Problems
    - 3 kHz and 10 kHz Resolution Bandwidth Problems
  - Step Gains
- Cal Oscillator Assembly (P/O A4)
  - Cal Oscillator Unlock at Beginning of IF Adjust

Inadequate CAL OSC AMPTD Range  
300 Hz to 3 kHz Resolution Bandwidth Out of Specification  
Low-Pass Filter  
Sweep Generator  
AM/FM Demodulation, Audio Amplifier, and Speaker

**Note** Because the cal oscillator circuitry on the A4 assembly is such an integral part of the IF adjustment, always check this assembly first, before checking the rest of the IF Section. A faulty cal oscillator can cause many apparent “faults” in the rest of the IF Section.

## Troubleshooting Using the TAM

When using Automatic Fault Isolation, the TAM indicates suspected circuits that need to be manually checked. Use Table 8-1 to locate the manual procedure. Table 8-2 lists assembly test connectors associated with each Manual Probe Troubleshooting test. Figure 8-1 illustrates the location of A4 and A5 test connectors. Figure 8-2 illustrates the levels and paths through the IF Section.



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**Figure 8-1. A4 and A5 Test Connectors**

**Table 8-1. Automatic Fault Isolation References**

| Suspected Circuit Indicated by Automatic Fault Isolation | Manual Procedure to Perform               |
|----------------------------------------------------------|-------------------------------------------|
| Check Cal Oscillator on A4 Assembly                      | Troubleshooting the Cal Osc with the TAM  |
| Check Input Switch on A5 IF Assembly                     | Troubleshooting A5 with the TAM           |
| Check Linear Amplifiers on A4 Assembly                   | Linear Amplifiers                         |
| Check Log Expand on A3 Interface Assembly                | Refer to “Log Expand” in this chapter     |
| Check Step Gains on A5 IF Assembly                       | Step Gains                                |
| Check Video Offsets on A4 Assembly                       | Video Offset ( <i>steps 1 through 4</i> ) |
| Check VIDEO OUT on A4 Assembly                           | Video Output                              |

## Troubleshooting the Log Amplifier with the TAM

Manual probe troubleshooting tests several dc bias points and signal path voltages. A dc bias is measured in the limiter and a fault here indicates a broken limiter stage. Signal path voltages are measured at the input, after the video amplifier in the linear path, after the offset and gain compensation circuits in the log path, and after the video offset.

The cal oscillator on A4 is used as an input to the log amp for the purpose of measuring gains. Faults in the signal path voltages indicate broken circuitry in prior stages. This technique locates dead stages, but might not report slightly degraded ones. Both +15 V and -15 V are measured. The revision code is on J11.

## Troubleshooting A5 with the TAM

Manual Probe Troubleshooting calculates stage bias-currents which test the operation of the IF chain. (This technique locates dead stages, but might not report slightly degraded ones.) DACs that are monitored are listed below:

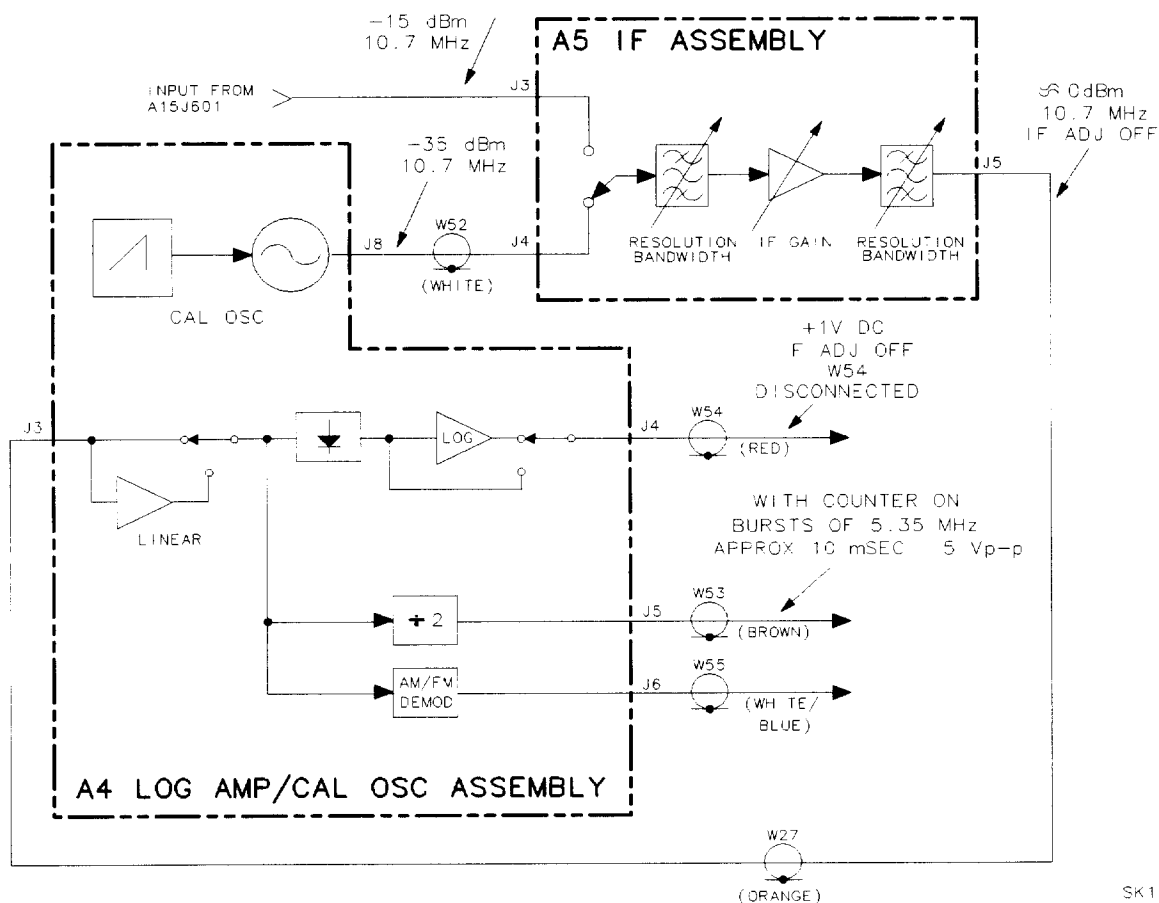
|        |             |
|--------|-------------|
| IFDAC1 | .....A5U812 |
| IFDAC2 | .....A5U813 |
| IFDAC3 | .....A5U809 |
| IFDAC4 | .....A5U807 |
| IFDAC5 | .....A5U810 |
| IFDAC6 | .....A5U806 |

**Table 8-2. TAM Tests versus Test Connectors**

| Connector | Manual Probe Troubleshooting Test | Measured Signal Lines |
|-----------|-----------------------------------|-----------------------|
| A3J105    | Video Input to Interface          | MS1                   |
|           | Video to Rear Panel               | MS2                   |
|           | Video MUX                         | MS3                   |
|           | Log Offset/Log Expand             | MS1,MS3               |
|           | Video Filter Buffer Amplifier     | MS3, MS5, OS1         |
|           | Video Peak Detectors              | MS5, MS6              |
|           | ADC MUX                           | MS6                   |
|           | Variable Gain Amplifier           | MS6, MS7              |
|           | Track and Hold                    | MS7, MS8              |
| A3J400    | Video Trigger DAC                 | MS1                   |
|           | Revision                          | MS2                   |
|           | Real Time DAC #1                  | MS3                   |
|           | RF Gain DACs                      | MS6                   |
|           | ADC Start/Stop Control            | MS7                   |
|           | Trigger                           | MS8                   |
| A4J9      | Cal Osc Sweep Gen Hardware        | MS1, MS2              |
|           | Cal Osc Tune Line Test            | MS3                   |
|           | Cal Osc ALC Test                  | MS4                   |
|           | Cal Osc Sweep Gen Output          | MS6                   |
| A4J10     | Log Amp Input Switch              | MS1                   |
|           | Log Amp Limiter Bias              | MS2                   |
|           | Positive 15 V Supply              | MS5                   |
| A4J11     | Logamp Linear Output              | MS2                   |
|           | Logamp Linear MUX Path            | MS2,MS3,MS8           |
|           | Logamp Log Output                 | MS3                   |
|           | Logamp Compensation               | MS3,MS4               |
|           | Logamp Log MUX Path               | MS4,MS8               |
|           | Logamp Video Offset               | MS8                   |
|           | –15 Volt Supply                   | MS7                   |
|           | Revision                          | MS5                   |
| A5J6      | 1st Step Gain Stage 1             | MS1, MS2, MS8         |
|           | 1st Step Gain Stage 2             | MS1, MS2, MS3         |
|           | 1st XTAL Pole Stage               | MS2, MS3, MS4         |
|           | 2nd XTAL Pole Stage               | MS3, MS4, MS5         |
|           | 1st LC Pole Stage 1               | MS4, MS5, MS6         |
|           | 1st LC Pole Stage 2               | MS5, MS6, MS7         |

**Table 8-2. TAM Tests versus Test Connectors (continued)**

| Connector | Manual Probe Troubleshooting Test | Measured Signal Lines |
|-----------|-----------------------------------|-----------------------|
| A5J7      | Ref 15 dB Attenuator Stage        | MS1, MS2, MS3         |
|           | 2nd Step Gain Stage               | MS2, MS3, MS4         |
|           | 2nd/3rd Step Gain Stage           | MS3, MS4, MS5         |
|           | 3rd Step Gain Stage               | MS4, MS5, MS6         |
|           | Fine Atten/3rd XTL Pole           | MS5, MS6, MS7         |
|           | 3rd XTAL Pole Stage               | MS6, MS7, MS8         |
| A5J8      | Revision                          | MS8                   |
|           | 4th XTAL Pole Stage               | MS1, MS2, MS3         |
|           | Post Amplifier Stage 1            | MS2, MS3, MS4         |
|           | Post Amplifier Stage 3            | MS3, MS4, MS5         |
|           | 3rd LC Pole Stage                 | MS5, MS6, MS7         |
|           | 4th LC Pole Stage                 | MS6, MS7              |
| A5J9      | IFDAC Channels 'A'                | MS1                   |
|           | IFDAC Channels 'B'                | MS3                   |
|           | IFDAC Channels 'C'                | MS4                   |
|           | IFDAC Channels 'D'                | MS2                   |
|           | Latched IF Control Lines          | MS5                   |
|           | Negative 15 V Supply              | MS6                   |
|           | 5 Volt Supply                     | MS7                   |
|           | 10 Volt Reference                 | MS8                   |



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**Figure 8-2. IF Section Troubleshooting with the TAM**

Both the digital control and DACs are multiplexed onto test point "channels" through resistive networks. One DAC from each of the quad-DAC packages feeds into a network. The TAM varies each DAC individually to isolate which ones failed. Similarly, 10 digitally-controlled lines feed into a network and are monitored by the TAM. The channels used to monitor the DACs are listed below:

|           |       |                  |
|-----------|-------|------------------|
| Channel A | ..... | A5J9 pin 1 (MS1) |
| Channel B | ..... | A5J9 pin 3 (MS3) |
| Channel C | ..... | A5J9 pin 4 (MS4) |
| Channel D | ..... | A5J9 pin 2 (MS2) |

1. On the HP 8560E, press **PRESET**, **MODULE**, and **Diagnose**. Select **Cal Osc Troubleshooting Mode**.
2. On the HP 8560E, disconnect W27 (coax 3) from A5J5 and monitor the output of A5J5 with a second spectrum analyzer.

3. Set the other spectrum analyzer controls as follows:

Span ..... 5 MHz  
Reference level ..... -20 dBm  
Center frequency ..... 10.7 MHz

4. On the HP 8560E, set the cal oscillator to 10.7 MHz by selecting **Fixed Tuned to 10.7 MHz**.
5. A -25 dBm signal from A5J5 should be displayed. If the signal is missing, disconnect W52 (coax 9) from A5J4. This is the cal oscillator signal input from the cal oscillator on the A4 assembly.
6. Connect the end of cable W52 to the input of the second spectrum analyzer. The signal coming from cable W52 should be -35 dBm at 10.7 MHz. If the cal oscillator signal from cable W52 is correct, the A5 IF assembly is probably at fault.

### Troubleshooting the Cal Oscillator with the TAM

1. Enter the TAM Cal Osc Troubleshooting Mode.
2. On the spectrum analyzer, disconnect cable W52 (coax 9) from A5J4 and connect this end of cable W52 to the input of a second spectrum analyzer.
3. Set the controls of the second spectrum analyzer connected to cable W52 to the following:

Span ..... 5 MHz  
Reference level ..... -30 dBm  
Center frequency ..... 10.7 MHz

4. Select each of the fixed-tuned frequencies. Verify at each frequency that the signal amplitude measures -35 dBm. If the frequency is incorrect, do the following:
  - a. Verify that the reference divider output (A4U811 pin 9) is 100 kHz. If it is not, verify that the 10 MHz reference is present at A4U811 pin 1.
  - b. Verify that the frequency found on the output of the divider (A4U808 pin 15) matches the output of the reference divider. Matching frequencies indicate the oscillator loop is locked. If the loop is not locked, troubleshoot the divider, oscillator, or phase detector.
  - c. Verify that the frequency found at the divider input (A4U808 pin 3) matches the CW frequency chosen in step a. Matching frequencies indicate a properly working oscillator. If the frequency is different, troubleshoot the divider.
  - d. Repeat step c for all the CW frequencies provided by the test.
5. Select each of the sweep widths (these sweeps are centered about 10.7 MHz).
6. Reduce the span of the other spectrum analyzer to check that the cal oscillator is actually sweeping. If the oscillator is not sweeping, perform the following steps:
  - a. The output of the sweep generator circuit (A4U804 pin 8 of function block Z) should be a series of negative-going parabolas (frequency and amplitude vary depending on the sweep width chosen). Table 8-3 lists the RANGE, MA0, and MA1 values for the sweep widths. If a failure is indicated in the IF/LOG CHECK, press **More Info** to provide more detailed information about the detected failure. If an HP-IB printer is available, connect it to the spectrum analyzer HP-IB connector, then press **Print Page** for a hard copy output.

**Table 8-3. Sweep Width Settings**

| Sweep Width | Sweep Time | Res BW<br>Adjusted | RANGE<br>A4U105<br>Pin 6 | MA1<br>A4U105<br>Pin 2 | MA0<br>A4U105<br>Pin 5 |
|-------------|------------|--------------------|--------------------------|------------------------|------------------------|
| 20 kHz      | 5 ms       | 10 kHz             | +5 V                     | 0 V                    | 0 V                    |
| 10 kHz      | 10 ms      | 3 kHz              | +5 V                     | 0 V                    | +5 V                   |
| 4 kHz       | 30 ms      | 1 kHz              | +5 V                     | +5 V                   | 0 V                    |
| 2 kHz       | 15 ms      | 300 Hz             | +5 V                     | +5 V                   | +5 V                   |

## Automatic IF Adjustment

The spectrum analyzer performs an automatic adjustment of the IF Section whenever needed.

The cal oscillator on the A4 assembly provides a stimulus signal which is routed through the IF during the retrace period.

The A3 Interface assembly measures the response using its analog-to-digital converter (ADC). The spectrum analyzer turns the cal oscillator off during a sweep.

When IF ADJ is ON, the spectrum analyzer readjusts part of the IF circuitry during each retrace period to readjust the IF completely every 5 minutes.

Automatic IF adjustment is performed upon the following conditions:

- **Power on:** (unless **STOP ALIGN** is pressed). The IF parameter variables are initialized to values loaded in program ROM and all possible IF adjustments are made. If **STOP ALIGN** is pressed, the adjustment is halted.
- If **REALIGN LO & IF** is selected: All possible IF adjustments (and LO adjustments) are made with the most recent IF parameter variables used as the starting point.
- If **FULL IF ADJ** is selected: All possible IF adjustments are made with the most recent IF parameter variables used as the starting point. ( **FULL IF ADJ** is located in the **CAL** menu.)
- If **ADJ CURR IF STATE** is selected: All amplitude data and some resolution bandwidths are adjusted. The bandwidths adjusted are a function of the currently selected resolution bandwidth setting.
- **Between sweeps:** IF ADJ must be set to ON. When IF ADJ is OFF, an **A** is displayed along the left side of the graticule.

If a FULL IF ADJ sequence cannot proceed beyond the amplitude portion, check the output of the cal oscillator on the A4 assembly as follows:

1. Disconnect cable W52 (coax 9) from A5J4. Connect cable W52 to the input of a second spectrum analyzer.
2. Set the second spectrum analyzer center frequency to 10.7 MHz and the reference level to -30 dBm.
3. On the HP 8560E under test, press **FULL IF ADJ** and observe the display of the second spectrum analyzer
4. If a -35 dBm signal does not appear, the cal oscillator is probably at fault.

### Parameters Adjusted

The following IF parameters are adjusted in the sequence listed:

1. Amplitude
  - A. Video Offsets: analog (using log amplifier video offset DAC) and digital (applying stored constant to all readings)
    1. Linear Scale Offset
    2. Log Scale Offset
      - a. Wideband and Narrowband modes.
      - b. 0 to 60 dB range in 10 dB steps.
      - c. 10 dB/DIV and 2 dB/DIV (log expand) modes.
  - B. Step Gains (A5 IF Assembly)
    1. First Step Gain for 16 different DAC settings.
    2. Second Step Gain for 16 different DAC settings.
    3. Third Step Gain for 0, 15, and 30 dB attenuation relative to maximum gain.
    4. Fine Attenuator for 32 evenly-spaced DAC settings.
  - C. Log Amplifier Slopes and Fidelity
    1. Wideband (RES BW 300 kHz through 2 MHz) and Narrowband modes (RES BW 300 Hz through 100 kHz)
    2. 10 dB/DIV and 2 dB/DIV (log expand) modes
  - D. Linear Scale Gains - On the log amplifier assembly (P/O A4)
  - E. Peak Detector Offsets (both Positive and Negative Peak Detectors with respect to normal sample path used by Auto IF Adjust)
2. LC Bandwidths
  - A. 300 kHz resolution bandwidth center frequency, bandwidth, and gain
  - B. 1 MHz resolution bandwidth center frequency, bandwidth, and gain
  - C. 2 MHz resolution bandwidth gain
  - D. 100 kHz resolution bandwidth center frequency, bandwidth, and gain
  - E. 30 kHz resolution bandwidth center frequency, bandwidth, and gain
  - F. Gain of all resolution bandwidth relative to the 300 kHz RES BW

### 3. Crystal Bandwidths

- A. The cal oscillator sweep rate is measured against the 100 kHz resolution bandwidth filter skirt. This result is used in compensating the sweeps used for adjusting the crystal bandwidths.
  - B. 10 kHz resolution bandwidth
    - 1. Center frequency of LC tank that loads the crystal
    - 2. Symmetry adjustment to cancel crystal case capacitance
    - 3. Bandwidth
  - C. 3 kHz resolution bandwidth: center frequency of LC tank and bandwidth of resolution bandwidth
  - D. 1 kHz resolution bandwidth: bandwidth
  - E. 300 Hz resolution bandwidth: bandwidth
  - F. Gain of all resolution bandwidth relative to the 300 kHz RES BW
4. Digital Bandwidths (1 Hz through 100 Hz; 10 Hz through 100 Hz if Option 103)
- A. VCXO (final LO) tuned to align digital bandwidths with crystal bandwidth center frequency
  - B. Overall gain
  - C. Gain variation with input frequency

### Requirements

For the Automatic IF Adjustment routine to work, the spectrum analyzer must provide the following basic functions:

- Power supplies
- Control signals
- ADC
- 10 MHz Frequency Reference to the A4 log amp/cal oscillator
- A15 RF Assembly isolation from the RF signal during IF adjustment

A15 RF assembly isolation is a function of the REDIR signal in the A15 Flatness Compensation Control block.

The references against which the Automatic IF Adjustment routine aligns are:

- 10 MHz reference (A15)
- Linear Scale Fidelity, especially the 10 dB gain stage in A4 Linear Amplifier block.
- 15 dB Reference Attenuator (A5)
- Cal Oscillator output power (A4)

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## Performance Test Failures

Failures in IF-Section-related performance tests may be investigated using the following information.

### IF Gain Uncertainty Performance Test

Failure of this performance test indicates a possible problem with the spectrum analyzer IF gain circuits. Assuming no major IF problems causing IF adjustment errors, IF gain problems in the first 50 dB of IF gain (REF LVLs of 0 dBm to -50 dBm with 10 dB ATTEN) are a result of faults on the A5 IF Assembly. IF gain problems in the next 60 dB of IF gain (REF LVLs of -60 dBm to -110 dBm, 10 dB ATTEN) result from log amplifier faults on the A4 assembly.

A signal level of -5 dBm is required at input (A5J3) for displaying a signal at top screen with 10 dB input attenuation and a 0 dBm reference level. Isolate IF gain problems on the log amplifier assembly (A4) with the following steps:

1. On the spectrum analyzer press **PRESET**, **SPAN**, **ZERO SPAN**, **FREQUENCY**, 1 **GHz**, **AMPLITUDE**, -50 dBm.
2. Press **CAL** and **IF ADJ OFF**.
3. Disconnect cable W27 (coax 3) from A5J5 and connect cable W27 to the output of a signal generator.
4. Set the signal generator controls as follows:  
Amplitude ..... +10 dBm  
Frequency ..... 10.7 MHz
5. Simultaneously decrease the signal generator output and the spectrum analyzer REF LVL in 10 dB steps. The signal displayed by the spectrum analyzer should remain at the reference level for each step. If the signal deviates from the reference level, troubleshoot the video offset circuitry on the A4 assembly.
6. Repeat steps 1 through 5 with the spectrum analyzer set to linear.

### Scale Fidelity Performance Test

Failure of this performance test indicates a possible problem with the A4 assembly.

- If the Linear, 5 dB/DIV, or 10 dB/DIV scales are out of specification, the fault is most likely on the log amplifier assembly (P/O A4).
- If only the 1 dB/DIV or 2 dB/DIV scales are out of specification, the fault is most likely on the A3 interface assembly.

## Resolution Bandwidths Performance Tests

Most resolution bandwidth problems are a result of A5 IF assembly failures. The resolution bandwidths are adjusted in the following sequence using 300 kHz as the reference: 1 MHz, 2 MHz, 100 kHz, 30 kHz, 10 kHz, 3 kHz, 1 kHz, 300 Hz, 100 Hz, 30 Hz, 10 Hz, 3 Hz, and 1 Hz. The 3 Hz and 1 Hz bandwidths are not available with Option 103.

If the IF adjustment routine encountered an error, the previously adjusted resolution bandwidths should be working properly and default DAC values are used for the remaining resolution bandwidth settings.

If the IF bandpass adjustments and the automatic IF adjustments fail to bring the resolution bandwidths within specification, troubleshoot the A5 IF assembly.

---

## Log Amplifier Assembly (P/O A4)

The log amplifier assembly on A4 performs several functions. It provides log and linear paths converting the 10.7 MHz IF signal to video. In addition it also provides offset circuitry, AM/FM demodulator circuitry, a frequency counter output, and down conversion of the 10.7 MHz IF to 4.8 kHz for use by the digital IF.

The log amp results are realized by using a wide dynamic range linear detector followed by a video log amp. The detector is used for both linear and log paths and contains a mixer that acts as the down converter mixer for the digital IF.

---

### Caution

For troubleshooting, it is recommended that you use an active probe, such as an HP 85024A, and another spectrum analyzer. If an HP 1120A active probe is being used with a spectrum analyzer having dc coupled inputs, such as the HP 8566A/B, HP 8569A/B and the HP 8562A/B, either set the active probe for an ac-coupled output or use a dc-blocking capacitor between the active probe and the spectrum analyzer input. Failure to do this can result in damage to the spectrum analyzer or the probe.

---

## Log Amplifier

Refer to function blocks K, L, and AE of A4 Log Amplifier Schematic Diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*. The log amplifier receives the detected video signal from the Detector/Mixer and outputs a voltage proportional to the log of the input voltage. The linear output is tapped off at the emitter of U501D. U507 provides input offset adjustment capability and adjusts the offset of the op amp formed by U501A, B, C, and D. Q502 is a buffer. Q501 switches in additional offset for digital RBWs. The logarithmic characteristic of the base-emitter junction of U502B is used in the feedback path to produce the logging affect. U502D is used to adjust for non-linearities in the linear mode. R531 is used to adjust log fidelity at the top of the screen.

Use the following steps to verify proper operation of the log amplifier chain:

1. Press **CAL** and **IF ADJ OFF**. Set the digital multimeter to read dc volts and connect the negative lead to the chassis of the spectrum analyzer.
2. Remove W27 from A4J3 and inject a 10.7 MHz signal of +10 dBm into A4J3.
3. Set the spectrum analyzer to log mode, with a resolution bandwidth of 300 kHz and single sweep.
4. Using the DMM, check the voltage at U503 pin 6.
5. Verify that this level is about -700 mV.
6. Adjust the source amplitude to place the signal at the reference level.
7. Reduce the input signal level in 10 dB steps, down to -60 dBm, while noting the voltage displayed on the DMM. The voltage should increase (become less negative) at a rate of 30 mV for each 10 dB decrease in input power. Troubleshoot the A4 assembly if the signal does not decrease properly.
8. Set the spectrum analyzer resolution bandwidth to 100 kHz to place the wide/narrow filter in narrow mode.
9. Repeat steps 2 through 7.
10. If log fidelity is poor near the bottom of the screen or the 1 MHz resolution bandwidth is narrow, a fault might exist in the wide/narrow filter switch. (Refer to function block G of A4 log amplifier schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.) Check this switch as follows:
  - a. Monitor voltages on A4U302 pins 1 and 7 while changing the spectrum analyzer resolution bandwidth from 100 kHz to 300 kHz.
  - b. If the voltages do not come within a few volts of the +15 V and -15 V supplies, U103 and U302 are suspect.
  - c. Disconnect the digital multimeter and reconnect W27 to A4J3.

## Linear Amplifiers

Refer to function block C of A4 log amplifier schematic diagram (sheet 2 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*. The Linear Amps consist of two variable gain stages, U201C and U201E as well as the buffer amplifier A4U201B, A4U201D, and A4Q201. The linear amplifiers provide 0 to 40 dB of IF gain in 10 dB steps. The gain of A4U201C can be increased by 20 dB by turning on A4CR201 and A4CR210 with the control line LIN\_20B. The gain of A4U201E can be increased by either 10 dB or 20 dB with the control lines LIN\_10 or LIN\_20A respectively. The gain can be selected by setting the spectrum analyzers reference level.

**IF Gain Application Guidelines (ATTEN=10 dB)**

| Power into A4J3 | Reference Level | Gain of A4U201C<br>(Pin 8 in; Pin 3 out) | Gain of A4U201E<br>(Pin 3 in; Pin 10 out) | Total Gain |
|-----------------|-----------------|------------------------------------------|-------------------------------------------|------------|
| +6 dBm          | -50 dBm         | 0 dB                                     | 0 dB                                      | 0 dB       |
| -4 dBm          | -60 dBm         | 0 dB                                     | 10 dB                                     | 10 dB      |
| -14dBm          | -70 dBm         | 0 dB                                     | 20 dB                                     | 20 dB      |
| -24 dBm         | -80 dBm         | 20 dB                                    | 10 dB                                     | 30 dB      |
| -34 dBm         | -90 dBm         | 20 dB                                    | 20 dB                                     | 40 dB      |

Total gain can be measured by injecting the specified power into A4J3 and measuring the total gain provided by A4U201C and A4U201E. The following procedure provides a means of troubleshooting the linear amplifiers.

1. On the spectrum analyzer, press **PRESET**, **SPAN**, **ZERO SPAN**, **CAL**, **IF ADJ OFF**, **FREQUENCY**, 1 **GHz**, **AMPLITUDE**, -50 dBm, **LINEAR**, **MORE**, **AMPTD UNITS**, **dBm**, and **AMPLITUDE**.
2. Disconnect W27 (coax 3) from A4J3 and connect the output of a signal generator to A4J3.
3. Set the signal generator controls as follows:
 

Amplitude ..... +6 dBm  
Frequency ..... 10.7 MHz
4. Simultaneously decrease the signal generator output and spectrum analyzer REF LVL in 10 dB steps to -90 dBm. At each step, the signal displayed on the spectrum analyzer should be within one division of the previous position.
5. If a problem exists, isolate it by comparing the actual gain of A4U201C and A4U201E with those listed in the above gain guidelines.
6. Reconnect W27 (coax 3) to A4J3.

## Video Offset

Refer to function block P of A4 log amplifier schematic diagram (sheet 3 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The circuit provides a programmable video offset, with a step size of 5 mV, from -300 mV to +900 mV.

1. On the spectrum analyzer, press **PRESET**, **SPAN**, **ZERO SPAN**, **FREQUENCY**, 1 **GHz**, **AMPLITUDE**, -50 dBm, **CAL**, **IF ADJ OFF**.
2. Disconnect W27 (coax 3) from A4J3 and connect a signal generator to A4J3.
3. Set the signal generator controls as follows:  
Amplitude ..... +10 dBm  
Frequency ..... 10.7 MHz
4. Simultaneously decrease the signal generator output and spectrum analyzer reference level in 10 dB steps down to -110 dBm. At each step, the signal displayed on the spectrum analyzer should be close to the reference level.
5. Reconnect W27 (coax 3) to A4J3 and cycle the spectrum analyzer power. Press **STOP REALIGN** when it appears.
6. On the spectrum analyzer, press **SWEEP**, **SINGLE**, **CAL**, and **IF ADJ OFF**.
7. The offset DAC, A4U102 pin 2, should now be at its default value of approximately +2.45 V. The voltage at U601 pin 3 should be approximately 0 V for a DAC output of 2.45 V.
8. If this default offset voltage is incorrect, DAC U102 is the most probable cause.

## Video Output

1. On the spectrum analyzer, press **PRESET**, **FREQUENCY**, 300 **MHz**, **SPAN**, 100 **Hz**, **AMPLITUDE**, -10 dBm, **SGL SWP**, **CAL** and **IF ADJ OFF**.
2. Connect the CAL OUTPUT to the INPUT 50 $\Omega$  connector.
3. Disconnect W54 (coax 2) from A4J4. Connect a short SMB to SMB cable from A4J4 to an SMB tee and connect W54 to the tee. Connect a test cable from the tee to the input of an oscilloscope.
4. Set the oscilloscope controls as follows:  
Amplitude scale ..... 200 mV/div  
Offset ..... +400 mV  
Coupling ..... dc  
Sweep time ..... 50  $\mu$ s/div
5. The oscilloscope should display a 4.8 kHz sine wave.
6. Disconnect the cable from the CAL OUTPUT and the INPUT 50 $\Omega$  connectors.
7. Set the resolution bandwidth to 2 MHz.
8. Broadband noise should be displayed on the oscilloscope from approximately +200 mV to +400 mV.

9. As the **REF LVL** is decreased in 10 dB steps from  $-10$  dBm to  $-70$  dBm, the noise displayed on the oscilloscope should increase in 100 mV increments. If this response is not observed, refer to "Step Gains" and "Video Offset" in this chapter.
10. Reconnect cable W54 to A4J4.

### Frequency Counter Prescaler/Conditioner

Refer to function block Q of A4 log amplifier schematic diagram (sheet 4 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The frequency counter prescaler/conditioner divides the frequency by two, and then attenuates it. The circuit consists of frequency divider (U703A) and an output attenuator. The frequency divider turns on only when the instrument is counting.

### AM/FM Demodulator

Refer to function block R of A4 Log Amplifier Schematic Diagram (sheet 4 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The demodulator circuitry on the log amplifier on A4 produces a low-level audio signal. This audio signal is then amplified by the audio amplifier on A4. The FM demodulator demodulates narrowband FM (5 kHz deviation) signals. The detector demodulates AM signals.

1. If demodulation problems occur when the spectrum analyzer is in the frequency domain, perform the Frequency Span Accuracy performance test and, if necessary, the YTO Adjustments procedure.
2. If an FM signal cannot be demodulated, perform the Demodulator Adjustment procedure. If the output of A4C707 cannot be adjusted as described in the Demodulator Adjustment procedure, troubleshoot the FM Demodulator or Audio MUX circuits on A4.

### 4.8 kHz IF Filters

Refer to function block N of A4 Log Amplifier Schematic Diagram (sheet 3 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

Problems with the 4.8 kHz filters can result in spurious signals appearing 2.88 kHz to 3.52 kHz above the frequency of the desired response. Also, **ERR 536 RBW <300** may occur when problems exist with the 4.8 kHz IF filters.

Measure the passband of the 4.8 kHz IF Filters as described in the following procedure.

1. On the spectrum analyzer, press **CAL**, **IF ADJ OFF**, **SPAN**, and 600 **Hz**.
2. Disconnect W27 from A4J3 and inject a 10.7 MHz signal of  $-20$  dBm into A4J3.
3. Fine-tune the frequency of the signal generator to center the signal on the screen. Set the signal generator to sweep one 2 kHz span about this center frequency. Press **SGL SWP** on the HP 8563E.
4. Set another spectrum analyzer, such as the HP 8566A/B, to 4.8 kHz center frequency and 2 kHz span.

---

**Caution** If a dc block is not used, damage to the HP 8566A/B results. The HP 8566A/B and many other spectrum analyzers have dc-coupled inputs and cannot tolerate dc voltages on their inputs.

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5. Connect the VIDEO OUTPUT (rear panel) of the spectrum analyzer through a 20 dB attenuator and dc block to the input of the HP 8566A/B. Set the sweep time of the HP 8566A/B to 10 seconds.
6. Set the HP 8566A/B to single trigger and press TRACE A **CLEAR-WRITE**. Trigger a sweep of the HP 8566A/B and the signal generator simultaneously. The HP 8566A/B shows the passband of the 4.8 kHz IF filters. The 3 dB bandwidth of the filters should be 1.2 kHz. The passband of the filters should be flat within 2 dB over 800 Hz.
7. Reconnect W27 (coax 3) to A4J3.

## 10.7 MHz IF Filters

1. Press **PRESET**, **FREQUENCY**, 300 **MHz**, **SPAN**, 600 **Hz**, **CAL**, and **IF ADJ OFF**.
2. Disconnect W29 (coax 7) from A5J3. Set the signal generator for a 10.7 MHz signal at -50 dBm and connect it to A5J3.
3. Fine tune the frequency of the signal generator to center the signal on the HP 8560E display. Set the signal generator to sweep one 2 kHz span about this center frequency.
4. On the HP 8560E, press **SGL SWP**.
5. Disconnect W27 (coax 3) from A5J5. Connect a test cable from A5J5 to the input of an HP 8566A/B.
6. Set the HP 8566A/B as follows:

|                  |          |
|------------------|----------|
| Center frequency | 10.7 MHz |
| Span             | 2 kHz    |
| Reference level  | +10 dBm  |
| Sweep            | Single   |
7. Press TRACE A **CLEAR-WRITE** on the HP 8566A/B.
8. Trigger a sweep on the signal generator and on the HP 8566A/B simultaneously. The HP 8566A/B should display a 3 dB bandwidth of approximately 500 Hz.
9. Reconnect W27 (coax 3) to A5J5 and W29 (coax 7) to A5J3.

## 4.8 kHz and 10.7 MHz IF Filters

1. On the HP 8560E, press **PRESET**, **FREQUENCY**, 300 **MHz**, **SPAN**, 600 **Hz**, **CAL**, and **IF ADJ OFF**.
2. Disconnect W29 (coax 7) from A5J3. Set the signal generator for a 10.7 MHz signal at -60 dBm and connect it to A5J3.
3. Fine tune the frequency of the signal generator to center the signal on the HP 8560E display. Set the signal generator to sweep one 2 kHz span about this center frequency.
4. On the HP 8560E, press **SGL SWP**.
5. Set the HP 8566A/B to 4.8 kHz center frequency and 2 kHz span.

---

**Caution**      Damage to the HP 8566A/B results if a dc block is not used. The HP 8566A/B and many other spectrum analyzers have dc-coupled inputs and cannot tolerate dc voltages on their inputs.

---

6. Connect the VIDEO OUTPUT (rear panel) of the spectrum analyzer through a 20 dB attenuator and dc block to the input of the HP 8566A/B. Set the sweep time of the HP 8566A/B to 10 seconds.
7. Set the HP 8566A/B to single trigger and press TRACE A **CLEAR-WRITE**. Trigger a sweep on the HP 8566A/B and on the signal generator simultaneously. The HP 8566A/B should show a 3 dB bandwidth of 600 Hz  $\pm$ 100 Hz.
8. Reconnect W29 (coax 7) to A5J3.

## 10.6952 MHz VCXO

Refer to function block E of A4 log amplifier schematic diagram (sheet 2 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The purpose of the 10.6952 MHz voltage-controlled crystal oscillator (VCXO) is to provide an LO for down-converting the peak of the 10.7 MHz IF filter's passband to 4.8 kHz. Since the peak of the passband of the 10.7 MHz IF filters is 10.7 MHz  $\pm$ 300 Hz, the frequency of the VCXO is between 10.6949 MHz and 10.6955 MHz. This frequency can best be measured at the collector of A4Q202.

The center frequency of the 300 Hz resolution-bandwidth filters and the 1 Hz to 100 Hz filters should differ no more than 10 Hz. If the center frequency is different by more than this, or if no signal is present in the 1 Hz to 100 Hz resolution-bandwidth settings, troubleshoot the 10.6952 MHz VCXO.

Error message **ERR 539** may occur if the VCXO is not oscillating. If problems exist with the VCXO control voltage, error messages **ERR 536** or **ERR 530** may occur.

Between sweeps the VCXO, at times, is turned off. To prevent the oscillator from turning off, press **PRESET**, **FREQUENCY**, 0.3 **GHz**, **SPAN**, 1 **kHz**, **SGL SWP**, **CAL**, and **IF ADJ OFF**.

## Input Switch

Refer to function block D of A4 Log Amplifier Schematic Diagram (sheet 2 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The input switch switches between log and linear modes. In addition it contains a 20 dB attenuator which is used only in digital resolution bandwidth settings. CR207, CR208, and CR209 form the input switch. CR205 and CR206 switch in R234 when in linear mode to maintain a constant impedance at J3. CR210, CR211, CR212, and CR221 switch the 20 dB attenuator in and out.

## LO Switch

Refer to function block F of A4 Log Amplifier Schematic Diagram (sheet 2 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The LO switch switches the limiter input between the 10.7 MHz path or the 10.6952 MHz VCXO path.

## Synchronous Detector

A wide dynamic range linear detector is realized by the limiter (block G), the isolation amplifier (block H), the LO amplifier (block I), and the detector/mixer (block J). The combination of these circuits form what is commonly known as a synchronous detector.

The input signal is split between two paths. One path flows through the isolation amplifier and the other path flows through the limiter and LO amplifier. The path flowing through the limiter generates the LO for the detector/mixer block. The path through the isolation amplifier drives the RF port.

To troubleshoot this group of circuits set the RBW to 300 kHz. Inject 10.7 MHz at +6 dBm into J3. Probe the gate of A4Q404 or A4Q405 with a scope. Look for a 0 to -3 V square wave. Decrease the input power from +6 dBm to -84 dBm in 10 dB steps. The square wave signal should remain unchanged. It is normal for the phase of the signal to jitter at the lowest signal levels.

The signals at the gates of A4Q404 and A4Q405 should be 180 degrees out of phase from each other. If they are not 180 degrees out of phase or one of the signals are not present, troubleshoot the LO Amplifier or the FET's in the mixer. If the signal is not a symmetrical square wave, troubleshoot the LO amplifier. If the signal drops out prematurely or is not present at all, troubleshoot the limiter or LO amplifier.

Repeat the procedure for an  $\text{RBW} \leq 100 \text{ kHz}$ . If the log amplifier works in the 300 kHz RBW but not in the narrower RBWs, troubleshoot the log narrow filter in the limiter or isolation amplifier. A4CR302 and A4CR303 are varactor diodes in the limiter filter and are used to tune the filter.

### **Limiter**

Refer to function block G of A4 Log Amplifier Schematic Diagram (sheet 2 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The limiter consists of 7 identical 20 dB gain stages. A “log narrow filter” is switched in for RBWs  $\leq 100$  kHz. This filter is switched in using the control lines NARROW between the 4th and 5th stages. During normal operation, the limiter serves to amplify even the smallest 10.7 MHz signals up to a level sufficient to drive the LO Amplifier and subsequent detector/mixer. This signal serves as the LO for the mixer circuitry.

### **Isolation Amplifier**

Refer to function block H of A4 Log Amplifier Schematic Diagram (sheet 3 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The isolation amplifier prevents LO port to RF port feedthrough in the mixer from feeding back to the input of the limiter and causing loop oscillations. In addition, the isolation amplifier matches the phase of the non-limited signal path to the phase of the limited signal path. The isolation amplifier should have a gain of about 4 dB and also has a “log narrow filter” that is switched with the control line NARROWB.

### **Detector/Mixer**

Refer to function block J of A4 Log Amplifier Schematic Diagram (sheet 3 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

Sum and difference frequencies are produced in the Detector/Mixer. The difference frequency produces video (dc to approximately 3 MHz), since the two signals are at the same frequency. During digital resolution bandwidths the two signals are separated by about 4.8 kHz.

### **Log Offset/Gain Compensation**

Refer to function blocks L and M of A4 Log Amplifier Schematic Diagram (sheet 3 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

#### **Log Offset Compensation**

The gain of A4U503 is set to unity, with A4R539 and A4R540 combining for a gain of 0.5. Therefore, the gain from A4U503 pin 3 to A4U508 pin 3 should be 0.5.

### Log Gain Compensation

The gain of A4U508 is nominally 6.8, measuring from pin 3 to pin 8. To check the log offset/gain compensation circuits inject a +10 dBm signal into J3 with the spectrum analyzer set to log mode. Measure A4U503 pin 3,  $V_{in}(1)$  and A4U508 pin 3,  $V_{out}(1)$  and record the results. Decrease the input level to -40 dBm and make the same measurements recording  $V_{in}(2)$  and  $V_{out}(2)$ .

The gain is then:

$$\frac{(V_{out}(1) - V_{out}(2))}{(V_{in}(1) - V_{in}(2))}$$

This gives an offset-independent gain measurement.

### Video MUX

The video MUX switches the video output between linear, log and 4.8 kHz IF (for digital RBWs). The demod video is an unused feature. The easiest way to troubleshoot this circuit is to look for blown FETs. Bad FETs are characterized by having significant gate current. Only one of the signal lines LIN\_VIDEO, IF\_VIDEO or LOG\_VIDEO should be high (+15 V) at any given time. The others should be low (-15 V). Also look for a voltage drop of several volts across the gate resistors R601, R605, R609, or R613 when in either the off or on state. This indicates gate current and thus a bad FET.

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## A5 IF Assembly

The input switch connects the IF to either the cal oscillator on the A4 assembly or the 10.7 MHz IF output from the A15 RF assembly. The automatic IF adjustment uses the cal oscillator on A4 at instrument turn-on and between sweeps to align the IF filters and step-gain amplifiers. During sweeps the input switch selects the 10.7 MHz IF output from A15. The LC filters are variable-bandwidth filters that provide resolution bandwidths from 30 kHz to 2 MHz. The automatic IF adjustment sets the bandwidths and center frequencies of each filter stage.

The crystal filters are variable-bandwidth filters that provide resolution bandwidths from 300 Hz to 10 kHz. The automatic IF adjustment sets the filter bandwidths and symmetry.

The step-gain amplifiers consist of the first step-gain stage, second step-gain stage, and third step-gain stage. These amplifiers provide gain when the spectrum analyzer reference level is changed. The amplifiers also provide gain range to compensate for variations in the IF filter gains, which change with bandwidth and environmental conditions, and band conversion loss in the front end. Fixed-gain amplifiers shift the signal levels to lower the noise of the IF chain.

The assembly has two variable attenuators. The fine attenuator provides the 0.1 dB reference level steps. The reference 15 dB attenuator provides a reference for automatic adjustment of the step-gain amplifiers and the log amplifier. The reference 15 dB attenuator also provides gain for changes in spectrum analyzer reference level.

Various buffer amplifiers provide a high-input impedance to prevent loading of the previous filter pole and a low-output impedance to drive the next filter pole.

Digital control signals from the W2 control cable, the “analog bus,” drive the control circuitry. At the beginning of each sweep the analog bus sets each control line for instrument operation. At the end of each sweep the analog bus sets each control line for the next portion of the automatic IF adjustment routine. IF adjustments continuously remove the effects of component drift as the spectrum analyzer temperature changes.

The assembly contains a reference limiting amplifier. This amplifier provides a known amount of limiting for the automatic IF adjustment routines. (Limiting occurs only during the automatic IF adjustment routines.) The LC34\_Short switches are open during sweeps. The current in the reference limiter is increased during sweeps to prevent limiting.

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|                |                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Caution</b> | For troubleshooting, it is recommended that you use an active probe, such as an HP 85024A, and another spectrum analyzer. If an HP 1120A active probe is being used with a spectrum analyzer having dc-coupled inputs, such as the HP 8566A/B, HP 8569A/B and the HP 8562A/B, either set the active probe for an ac-coupled output or use a dc-blocking capacitor between the active probe and the spectrum analyzer input. |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

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|                |                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Caution</b> | <ul style="list-style-type: none"><li>■ Do not short control voltages to ground. These voltages are not short-circuit protected. DACs damaged by shorting these voltages might not fail until several weeks after the shorting takes place.</li><li>■ Do not short power-supply voltages to ground. The spectrum analyzer power-supply current limiting cannot protect the resistors in series with the power supply.</li></ul> |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

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**Note**                      Some transistors have collectors connected to the case. Electrical connection of the case to the collector might not be reliable, making collector voltage measurements on the transistor case unreliable.

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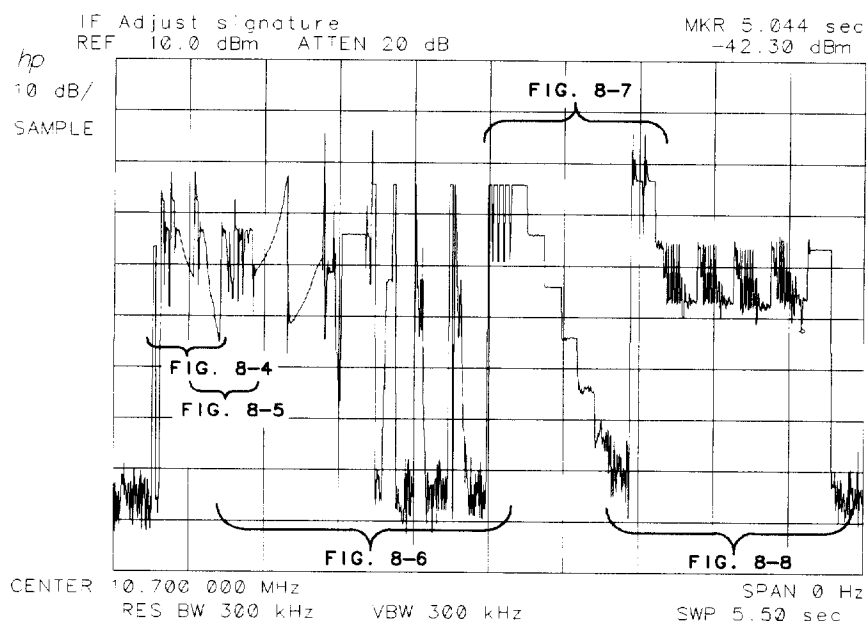
## IF Signature

1. Disconnect W27 (coax 3) from A5J5.
2. Connect an SMB tee to A5J5, using a short coaxial cable with SMB connectors.
3. Connect one output of the tee to cable W27 (coax 3).
4. Connect an HP 85024A active probe, with a 10:1 divider installed, to the other output of the tee.
5. Connect the output (type N connector) of the active probe to the input of the HP 8566A/B spectrum analyzer.
6. Connect the probe power cable to the HP 8560E front-panel PROBE POWER connector (you may need to use a probe power extension cable, HP 10131B).
7. Set the HP 8566A/B controls as follows:

|                            |          |
|----------------------------|----------|
| Reference level .....      | +10 dBm  |
| Center frequency .....     | 10.7 MHz |
| Span .....                 | 0 Hz     |
| Resolution bandwidth ..... | 300 kHz  |
| Video bandwidth .....      | 300 kHz  |
| Sweep time .....           | 5.5 s    |
| Trigger .....              | Single   |
8. On the HP 8566A/B, press **SHIFT**, (trace A blank) to set detector to SAMPLE mode.
9. On the HP 8560E, press **PRESET** and set the controls as follows:

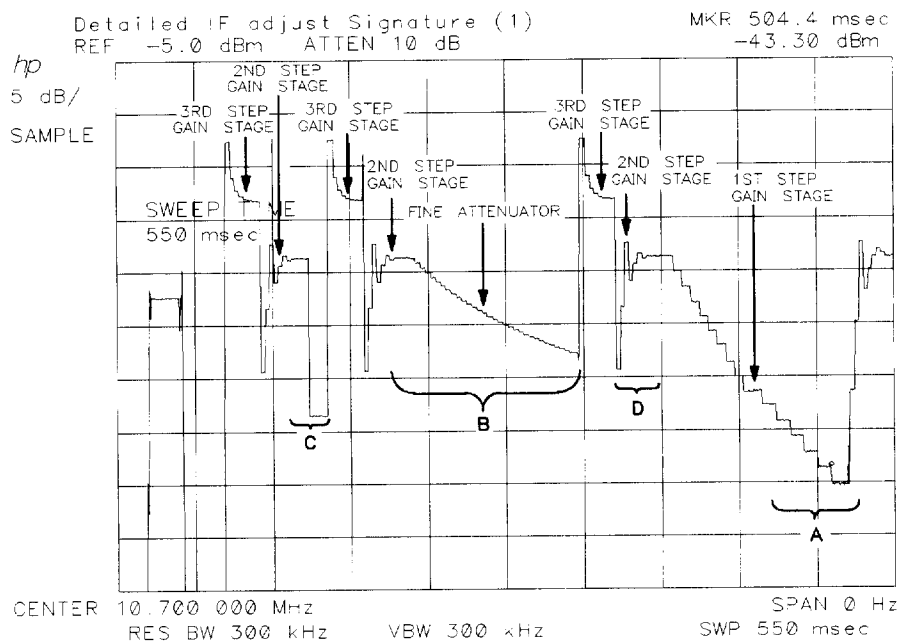
|                        |         |
|------------------------|---------|
| Center frequency ..... | 300 MHz |
| Span .....             | 5 MHz   |
10. On the HP 8560E, press **SGL SWP** and **CAL**.
11. Simultaneously press **SINGLE** on the HP 8566A/B and **ADJ CURR IF STATE** on the HP 8560E. The IF signature is displayed on the HP 8566A/B display. It may be necessary to experiment with different time intervals between initiating the sweep on the HP 8566A/B and initiating the current IF state adjustment on the HP 8560E.

12. Compare the IF signature to the signature of a properly operating spectrum analyzer illustrated in Figure 8-3. If the signatures do not closely resemble each other, a more detailed view of the signature may show the failed hardware.
  - a. Set the HP 8566A/B controls as follows:
    - Sweep time ..... 550 ms
    - dB/DIV ..... 5 dB
    - Reference level ..... -5 dBm
  - b. Press **SINGLE** on the HP 8566A/B and, a very short time later, press **ADJ CURR IF STATE** on HP 8560E. Figure 8-4 through Figure 8-8 illustrate detailed IF signatures of a properly operating HP 8560E. It may be necessary to experiment with different time intervals between initiating the sweep on the HP 8566A/B and initiating the current IF state adjustment on the HP 8560E to obtain the waveforms shown. Note the changes in the HP 8566A/B video bandwidth and sweep time.
13. Reconnect W27 (coax 3) to A5J5.



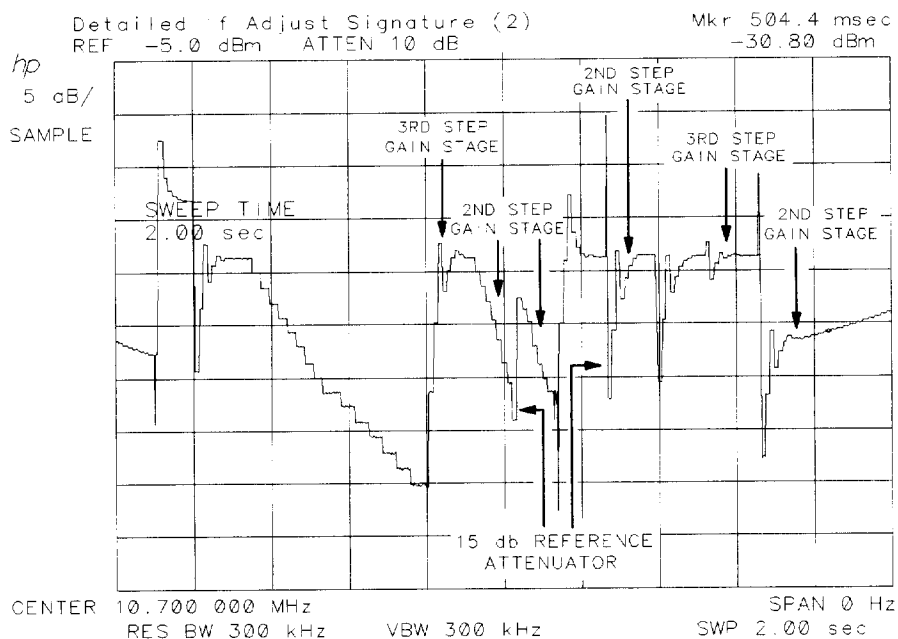
sp143e

**Figure 8-3. IF Adjust Signature**



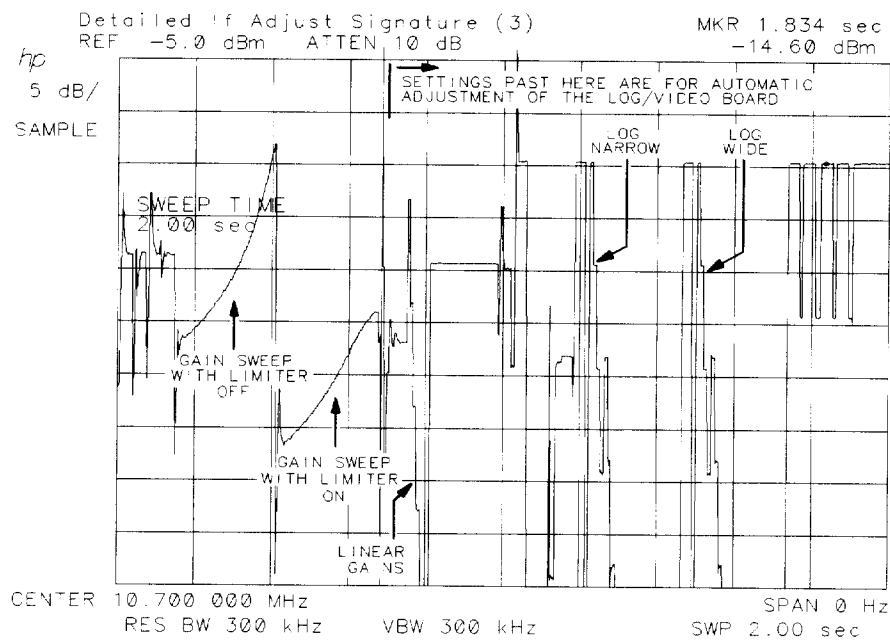
sp144e

**Figure 8-4. Detailed IF Adjust Signature (1)**



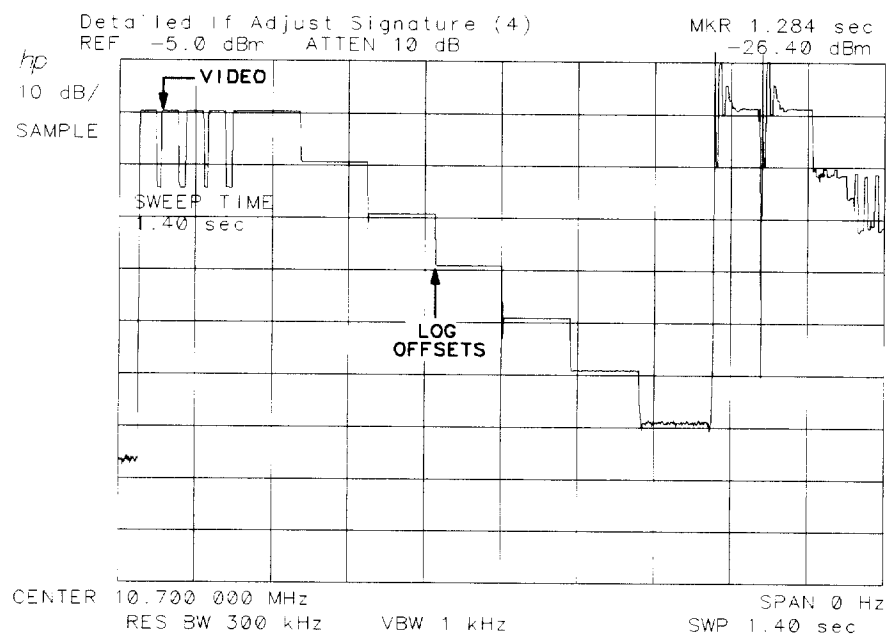
sp145e

**Figure 8-5. Detailed IF Adjust Signature (2)**



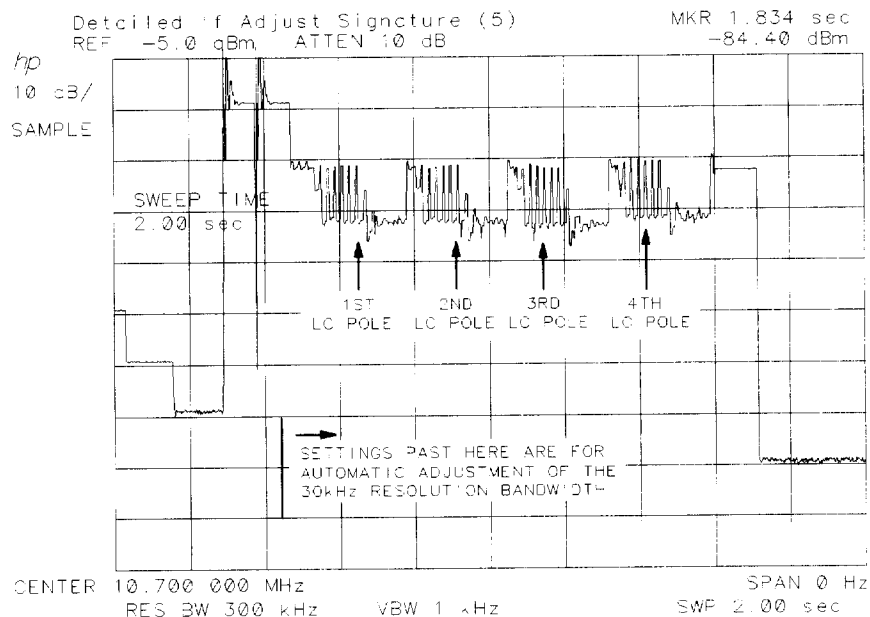
sp146e

Figure 8-6. Detailed IF Adjust Signature (3)



sp147e

Figure 8-7. Detailed IF Adjust Signature (4)



sp1489

**Figure 8-8. Detailed IF Adjust Signature (5)**

## Common IF Signature Problems

**Region A of Figure 8-4 is noisy:**

Suspect the first LC pole.

**Region B of Figure 8-4 is flat:**

Suspect the third step-gain stage, the fine attenuator, or the fourth LC-pole output amplifier.

**Region C of Figure 8-4 has no 15 dB step:**

Suspect the reference 15 dB attenuator.

**Region D of Figure 8-4 is flat:**

Suspect the second step-gain stage.

**Entire signature noisy:**

If the signature resembles Figure 8-9, suspect a broken first step-gain stage or a break in the signal path in the input switch, first crystal pole, or second crystal pole.

**Correct shape but noisy:**

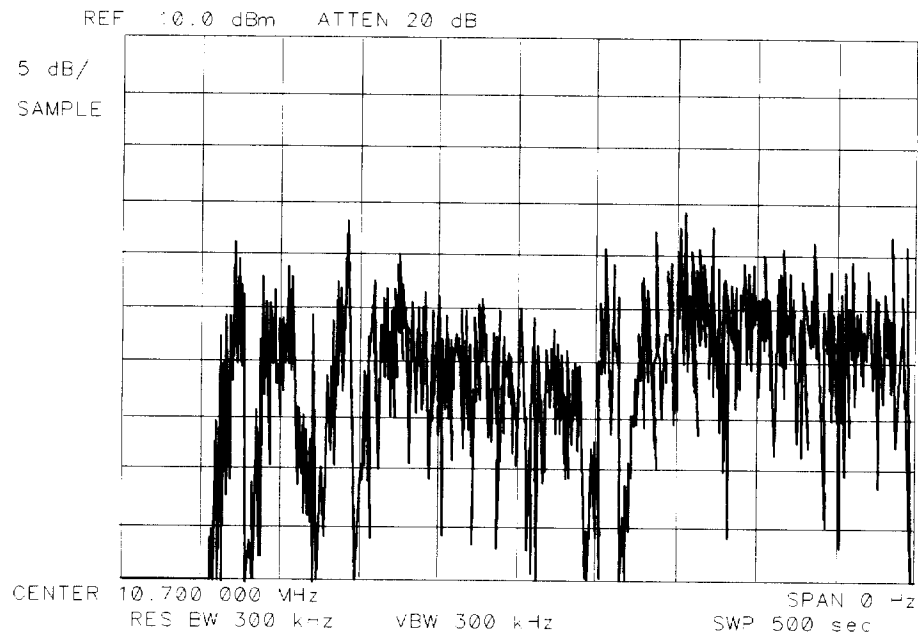
If the signature resembles Figure 8-10, suspect the second crystal-pole output amplifier.

**Amplitude of Region B of Figure 8-11 varies more than 12 dB:**

Suspect the third step-gain stage output amplifier.

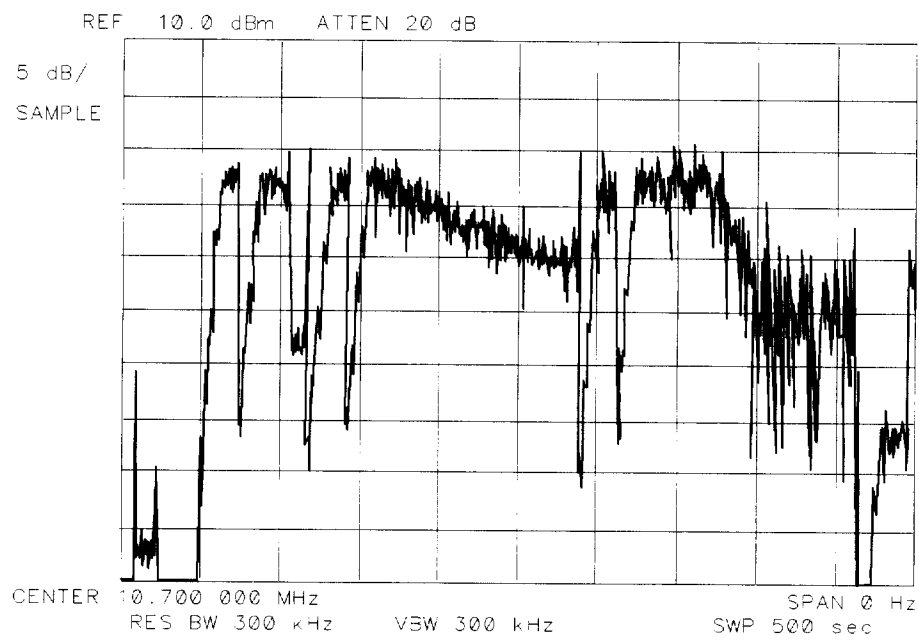
**Region B of Figure 8-12 is kinked:**

Suspect the fourth LC-pole output amplifier.



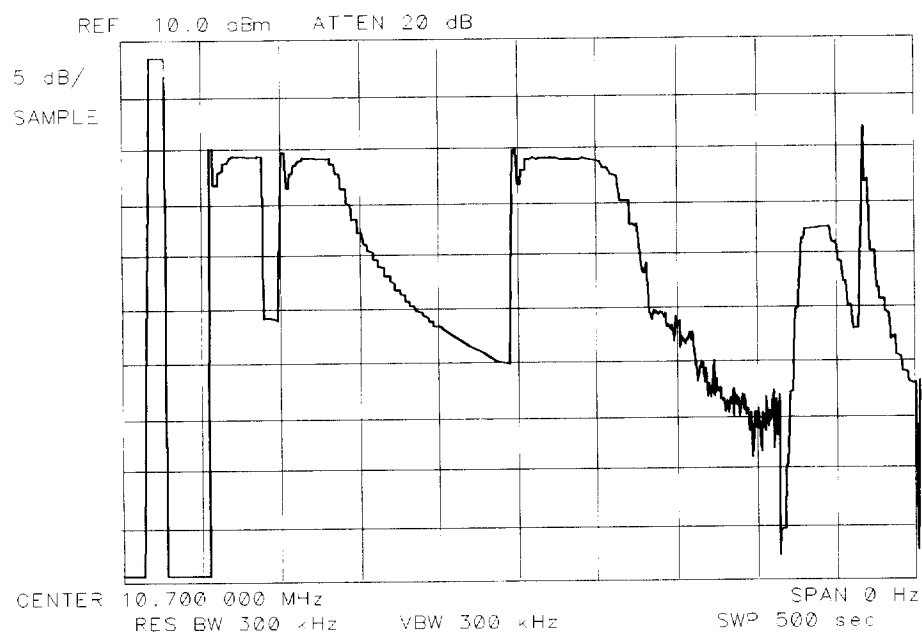
SK178

**Figure 8-9. Noisy Signature**



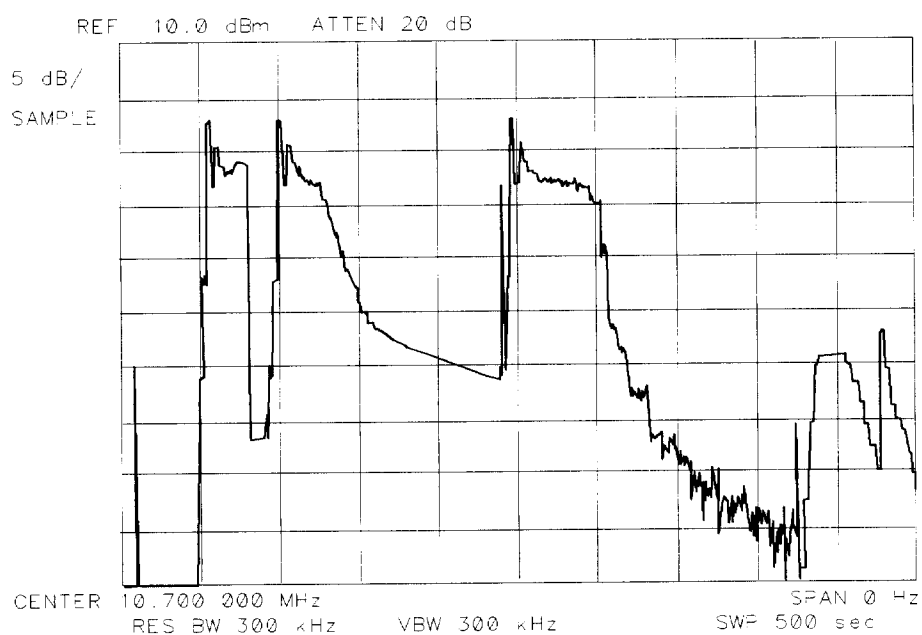
SK179

**Figure 8-10. Noise with Correct Shape**



SK180

**Figure 8-11. Region B Amplitude Variation**



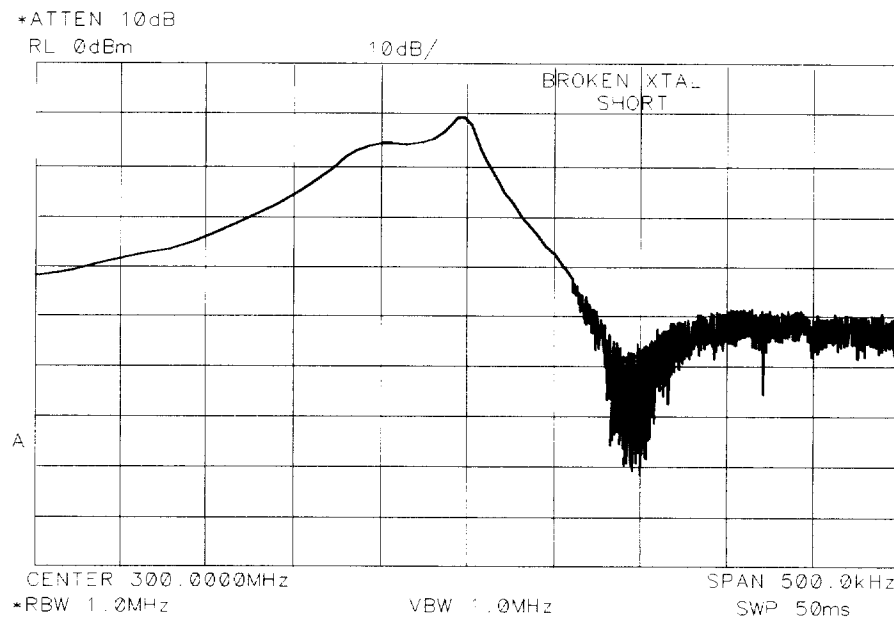
SK181

**Figure 8-12. Region B Amplitude Offset**

## 1 MHz Resolution Bandwidth Problems

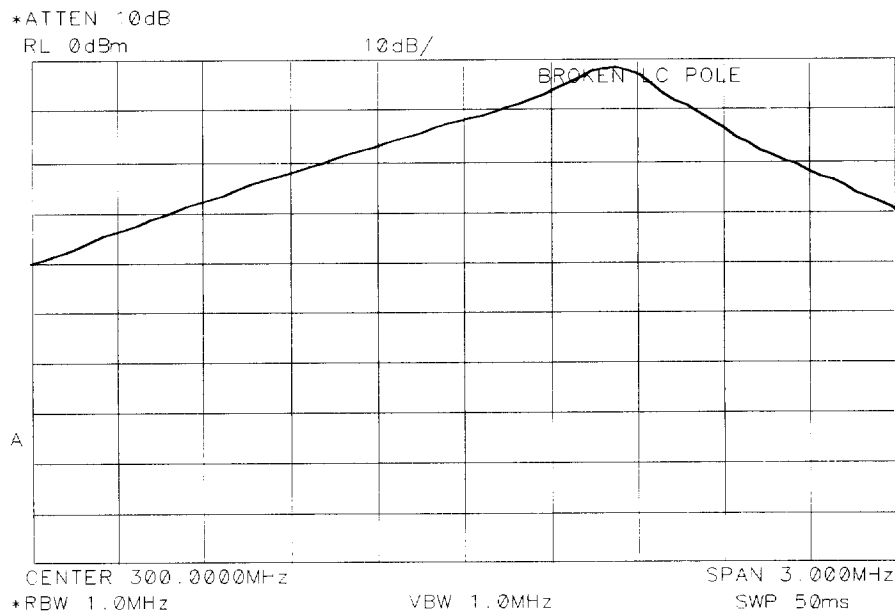
Check the crystal shorting switches as follows:

1. On the spectrum analyzer, press **PRESET** and set the controls as follows:  
Resolution bandwidth ..... 1 MHz  
Span ..... 500 kHz  
Center frequency ..... 300 MHz
2. On the spectrum analyzer, connect the 300 MHz CAL OUTPUT to the INPUT 50Ω.
3. If the trace flatness is not within 2.5 dB, a failure probably exists.
4. A trace similar to Figure 8-13 indicates a crystal short failure.
5. Press **SPAN** to set the spectrum analyzer to 3 MHz. A trace that slopes across the screen (see Figure 8-14) indicates a failed LC pole. To isolate the broken pole refer to the shape factor information in "30 kHz Resolution Bandwidth Problems."



SK 182

**Figure 8-13. Faulty Crystal Short**



SK 183

**Figure 8-14. Faulty LC Pole**

### 30 kHz Resolution Bandwidth Problems

**Shape factor too high:** Shape factor is the ratio of the 60 dB bandwidth to the 3 dB bandwidth. Shape factor should be less than 15:1. If one of the LC poles malfunctions, the shape factor may be the only indication of the failure. Isolate the non-functioning pole with the IF signature. Region E of Figure 8-8 illustrates the four LC- pole adjustments. Take several signatures to examine the LC-pole adjustments. If one of the four sections of Region E is consistently longer than the others, the corresponding LC pole is faulty.

**IF gain compression:** FET transistors Q301, Q303, Q700, and Q701 can deteriorate with age. Measuring less than 0 volts on the FET source indicates a bad FET.

**Bandwidth too wide:** Check for contamination on the printed-circuit board. Clean the board as required.

### 3 kHz and 10 kHz Resolution Bandwidth Problems

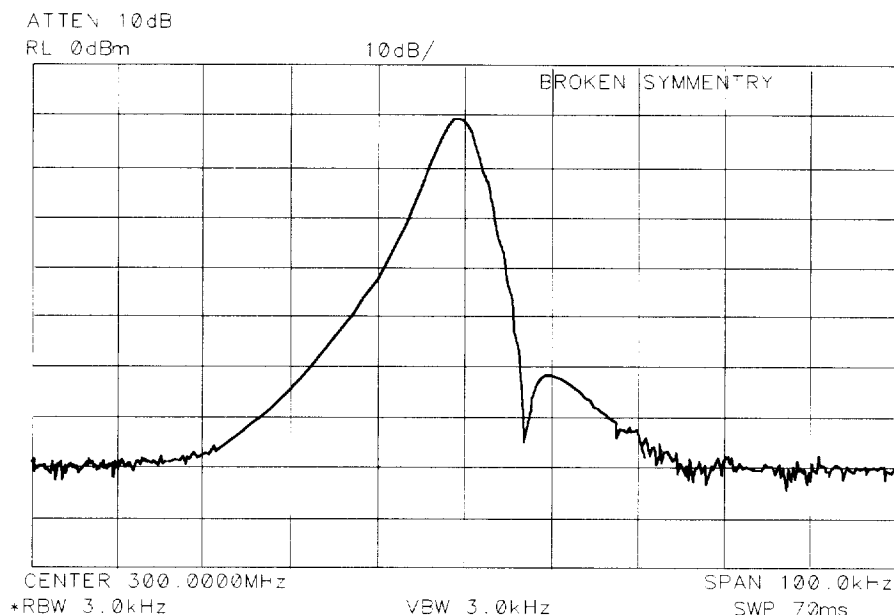
**Asymmetric Filter Response:** Check the crystal symmetry control with the following steps.

1. Press **PRESET**.
2. Set the spectrum analyzer controls as follows:
 

|                            |         |
|----------------------------|---------|
| Resolution bandwidth ..... | 3 kHz   |
| Span .....                 | 100 kHz |
| Center frequency .....     | 300 MHz |
3. On the spectrum analyzer, connect the 300 MHz CAL OUTPUT to the INPUT 50Ω.
4. A trace similar to Figure 8-15 indicates a failed crystal-symmetry circuit.

**Narrow 10 kHz resolution bandwidth:** Check for printed-circuit board contamination. Clean the board as required.

**IF Gain Compression in 10 kHz resolution bandwidth:** FET transistors Q202, Q203, Q501, and Q503 can deteriorate with age. Measuring less than 0 volts on the FET source indicates a bad FET.



SK184

**Figure 8-15. Faulty Crystal Symmetry**

## Step Gains

Refer to function blocks B, H, and I of A5 IF filter schematic diagram (sheets 1 of 3 and 2 of 3) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

1. On the spectrum analyzer, press **PRESET**, **SPAN**, **ZERO SPAN**, **FREQUENCY**, and 1 **GHz**.
2. Press **CAL** and **IF ADJ OFF**.
3. Disconnect W29 (coax 7) from A5J3 and W27 (coax 3) from A5J5.
4. Inject a -5 dBm, 10.7 MHz signal into A5J3.
5. Monitor the output of A5J5 with another spectrum analyzer.
6. Simultaneously decrease the signal generator output and spectrum analyzer reference level in 10 dB steps down to a -50 dBm reference level.
7. At each step, the signal displayed on the other spectrum analyzer should be close to +10 dBm. (More subtle IF gain problems might require smaller signal generator and reference level steps.)
8. Reconnect W29 to A5J3 and W27 (coax 3) to A5J5.

---

## Cal Oscillator Assembly (P/O A4)

The cal oscillator on the A4 assembly supplies the stimulus signal for automatic IF adjustments. Normally, the oscillator operates only during retrace (for a few milliseconds) to adjust part of the IF. (All IF parameters are to be readjusted about every 5 minutes.) With continuous IF adjust ON, a group of IF parameters are adjusted during each retrace period (non-disruptive). If continuous IF adjust is OFF, the most recent IF calibration data is used.

The IF parameters adjusted include step gains, log amplifier gain and offset, bandwidth centering, 3 dB bandwidth, bandwidth amplitude, and crystal-filter symmetry.

The cal oscillator provides three types of output signals (all  $-35$  dBm):

- 10.7 MHz
- 9.9 to 11.5 MHz in 100 kHz steps
- Frequency sweeps from 20 kHz to 2 kHz centered at 10.7 MHz (lasting 5 to 60 ms respectively)

The signals perform the following functions:

- Adjust gains, log amps, and video slopes and offsets.
- Adjust 3 dB bandwidth and center frequencies of LC resolution bandwidth filters (30 kHz through 1 MHz).
- Adjust 3 dB bandwidth, symmetry, and gain of the crystal resolution bandwidth filters (300 Hz through 10 kHz).

The cal oscillator uses a phase-locked loop (PLL). The oscillator (function block X) is locked to the instrument 10 MHz reference. The reference divider (function block U) divides the reference and delivers a 100 kHz TTL signal to the phase detector (function block V). The divide-by-N circuitry (function block Y) divides the oscillator output of 9.9 MHz to 11.5 MHz (by 99 to 115) resulting in a 100 kHz output to the phase detector. When the cal-oscillator PLL is locked, narrow positive and negative of equal width pulses occur at the phase detector output. Since the phase detector drives a low-input impedance at the loop integrator, observe the positive pulses at A4CR808 anode and negative pulses at A4CR809 cathode.

The loop integrator acts as a low-pass filter that filters the pulses and inverts the result. If the anode of A4CR808 is more positive (with respect to ground) than the cathode of A4CR809 is negative, the loop integrator output should saturate to approximately  $-13$  V. Conversely, if the anode of A4CR808 is less positive than the cathode of A4CR809 is negative, the integrator should saturate to a positive voltage.

---

|             |                                                                                                                                                                   |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note</b> | If error messages <b>ERR 581 AMPL</b> or <b>ERR 582 AMPL</b> appears, refer to error message <b>ERR 582 AMPL</b> in Chapter 6 and perform the procedure provided. |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|

---

1. The oscillator output frequency should exceed 11.5 MHz if the CAL OSC TUNE line, A4U804 pin 14, exceeds  $+9$  V. The oscillator frequency should be less than 9.9 MHz if CAL OSC TUNE is below  $-9$  V. The oscillator only operates when CALOSC\_OFF is low (0 V).
2. If the cal oscillator remains locked (no error code **ERR 499** displayed) but does not have the correct output level, troubleshoot the output leveling circuitry (function blocks AA, AB, and AC) or output attenuator (function block AD).

## Cal Oscillator Unlock at Beginning of IF Adjust

1. Press **LINE** to turn the spectrum analyzer off and then on. The words **IF ADJUST STATUS** appear on the display 10 seconds after the instrument is turned on (assuming the rest of the instrument is working correctly). Immediately observe the lower right corner of the display for error messages. If the message **ERR 499 CAL UNLK** appears (before errors **ERR 561**, **ERR 562** and **ERR 565**), the cal oscillator is unable to phase-lock. Expect to see the **ERR 499** message for only about 1 second.
2. If the spectrum analyzer registers an unlocked cal oscillator, continue with step 3 to verify the presence of externally supplied signals.
3. Check A4U811 pin 9 for a 100 kHz TTL-level square wave verifying operation of A4U811, A4Q802, and the 10 MHz input signal from A4J7.
4. Check the +15 VF, +5 VF and -15 V power supplies, and +10 V reference on the A4 assembly.
5. Check that A4U807 pin 5 (CALOSC\_OFF) becomes TTL low (0 V) at the start of a **FULL IF ADJ** (press **CAL** and **FULL IF ADJ**). The phase modulation output at A4U804 pin 8 should also remain at 0 volts. If these checks are correct, troubleshoot blocks V, W, X, and Y. See Figure 8-21, A4 Log Amplifier/Cal Oscillator Block Diagram (2 of 2).

## Inadequate CAL OSC AMPTD Range

Refer to function block AC of A4 Log Amplifier Schematic Diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

1. If A4R826, CAL OSC AMPTD, has inadequate range to perform the IF Amplitude Adjustment, press **CAL**.
2. Rotate A4R826 fully clockwise and disconnect W52 (coax 9) from A5J4.
3. Connect A5J4 to the input of a second spectrum analyzer.
4. Set the other spectrum analyzer controls as follows:

|                  |          |
|------------------|----------|
| Center frequency | 10.7 MHz |
| Reference level  | -30 dBm  |
5. Observe the spectrum analyzer display while pressing **FULL IF ADJ**. The signal level should be above -34.55 dBm. If the signal level is incorrect, continue with step 7.
6. Rotate A4R826 fully counterclockwise. The signal should be below -36.25 dBm. If the signal level is correct at both settings, troubleshoot the A5 IF assembly. If the signal level is incorrect, continue with step 7.
7. Troubleshoot the ALC loop on this assembly using the following steps:
  - a. Connect a positive DVM probe to A4J9 pin 4.
  - b. On the spectrum analyzer, press **CAL**.
  - c. Press **FULL IF ADJ**. Observe the DVM reading between the displayed messages **IF ADJUST STATUS: 300 kHz RBW** and **IF ADJUST STATUS: 3 kHz RBW**. During this time period, the voltage should be within a 2 to 10 Vdc range.
  - d. Observe the DVM reading while **IF ADJUST STATUS: AMPLITUDE** is displayed. The reading should be within the 2 to 10 Vdc range.

- e. If the DVM reading is outside the range in step c but inside the range in step d, suspect one of the filter's reactive components.
8. If the ALC loop is working correctly (A4J9 pin 4 within the test tolerances given), then either the output attenuator is defective, or A4U810 pin 6 (in ALC loop integrator) is outside of its +3 to +6 Vdc range.
9. Reconnect W52 (coax 9) to A5J4.

### 300 Hz to 3 kHz Resolution Bandwidth Out of Specification

1. If the 3 dB bandwidth of one of these filters is incorrect, suspect a failure of one of the five available sweeps from the cal oscillator's sweep generator (function block Z). These sweeps are generated by changing the switch settings of A4U803 which routes signals through A4U802 and A4U804.
2. Disconnect W52 (coax 9) from A4J8.
3. Connect the source connection of a 3 dB power splitter (Minicircuits Model: ZSC J-2-1) to A4J8. Connect one output of the power splitter to the input of an HP 8566A/B spectrum analyzer. Connect the other output of the power splitter to cable W52 (coax 9).

---

**Note** If a 3 dB power splitter is not available, an SMB tee and an active probe may be substituted. Connect the active probe between the tee and the other spectrum analyzer. The absolute power levels are approximately 3 dB higher than those stated below, due to the elimination of the 3 dB power splitter.

---

4. Press **INSTR PRESET** on the HP 8566A/B and set the controls as follows:
 

|                      |          |
|----------------------|----------|
| Center frequency     | 10.8 MHz |
| Span                 | 0 Hz     |
| Reference level      | -43 dBm  |
| Resolution bandwidth | 100 kHz  |
| Video bandwidth      | 10 kHz   |
| Sweep time           | 50 ms    |
| Scale                | 1 dB/DIV |
| Sweep                | Single   |
5. On the spectrum analyzer, press **PRESET** and **CAL**.
6. Press **FULL IF ADJ**. When the display reads **ADJUSTING IF: 10 kHz RBW**, press **SINGLE** on the HP 8566A/B.
7. The HP 8566A/B screen illustrates frequency versus time of the cal oscillator's output sweeps. See Figure 8-16. The slope of the HP 8566A/B 100 kHz resolution bandwidth is used to detect frequency changes. Sweeps that vary (greater than 30%) from the normal levels, trigger error code **ERR 581** or **ERR 582**.
8. Press **FULL IF ADJ**. When the display reads **ADJUSTING IF: 3 kHz**, press **SINGLE** on the HP 8566A/B.
9. Figure 8-17 illustrates normal operation. Severe failures (slope error greater than 30 percent) and subtle 3 kHz resolution bandwidth errors (less than 30 percent) indicate a problem with A4U802, A4U803, A4U804, or A4U106.

10. Severe failure of the bandwidth accompanied by subtle errors in the output signal indicate an A5 failure.
11. Set the HP 8566A/B controls as follows:
 

|                            |            |
|----------------------------|------------|
| Center frequency .....     | 10.710 MHz |
| Resolution bandwidth ..... | 10 kHz     |
| Video bandwidth .....      | 1 kHz      |
| Sweep time .....           | 200 ms     |
12. On the spectrum analyzer, press **FULL IF ADJ.** When the message **IF ADJUST STATUS: 1 kHz RBW** appears, press **(SINGLE)** on the HP 8566A/B.
13. Figure 8-18 illustrates normal operation. Severe failures (slope error greater than 30%) and subtle 3 kHz resolution bandwidth errors (less than 30%) indicate a problem with A4U802, U803, U804, or U106.
14. On the spectrum analyzer, press **FULL IF ADJ.** When the message **IF ADJUST STATUS: 300 Hz RBW** appears, press **(SINGLE)** on the HP 8566A/B.
15. Figure 8-19 illustrates normal operation. Severe failures (slope error >30%) and 3 kHz resolution bandwidth errors (less than 30%) indicate a problem with A4U802, U803, U804, or U106.
16. Reconnect W52 (white) to A4J8.

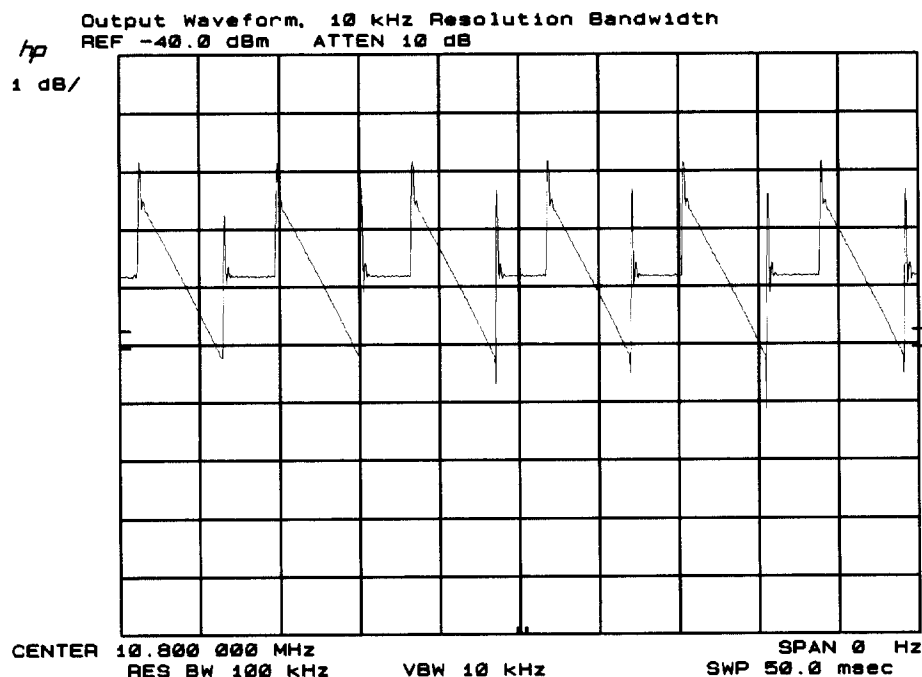


**Figure 8-16. Output Waveform, 10 kHz Resolution Bandwidth**

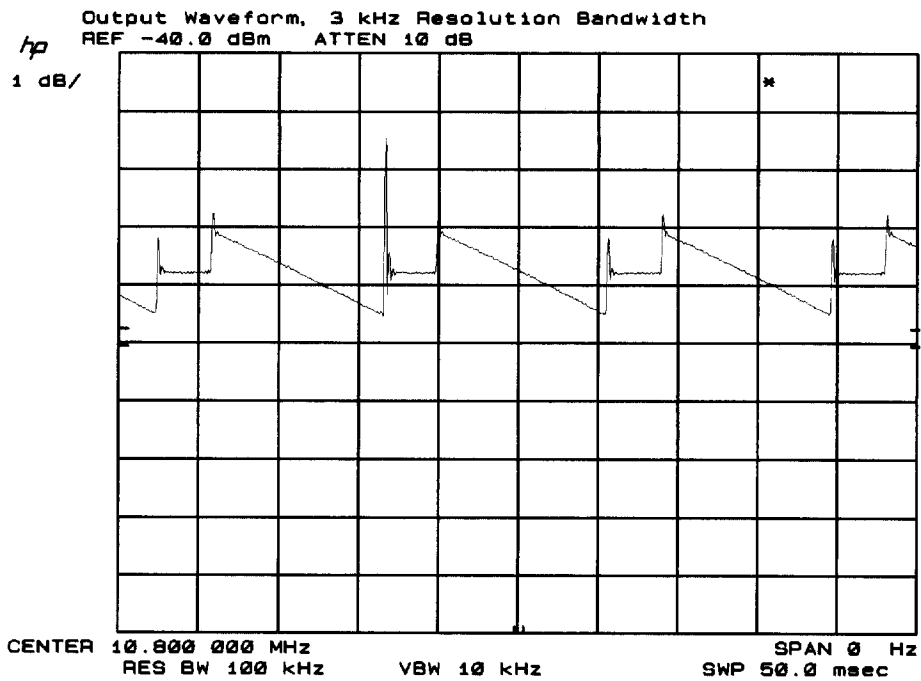


Figure 8-17. Output Waveform, 3 kHz Resolution Bandwidth

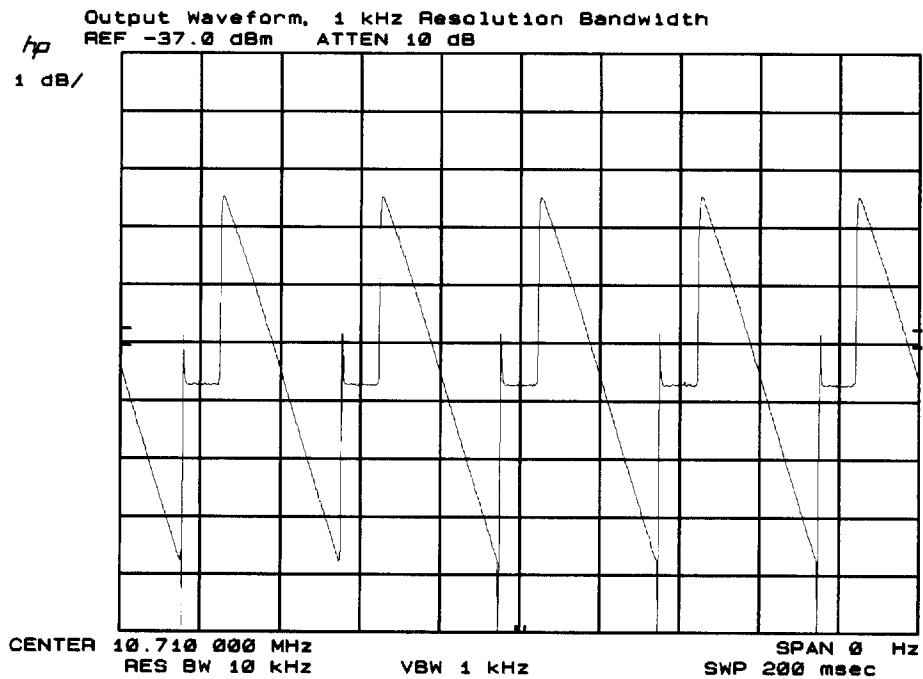


Figure 8-18. Output Waveform, 1 kHz Resolution Bandwidth

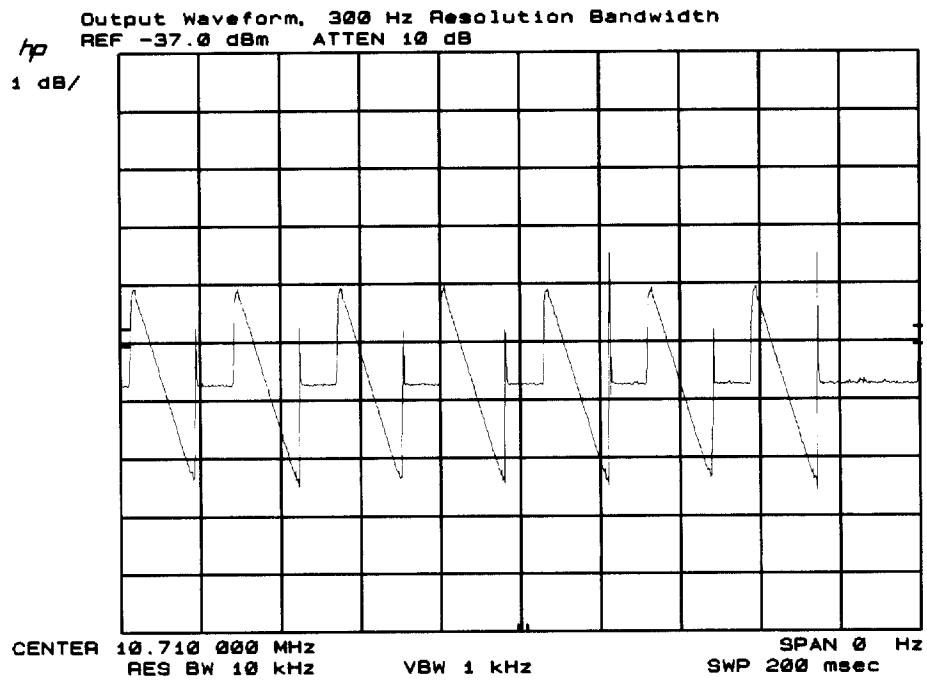


Figure 8-19. Output Waveform, 300 Hz Resolution Bandwidth

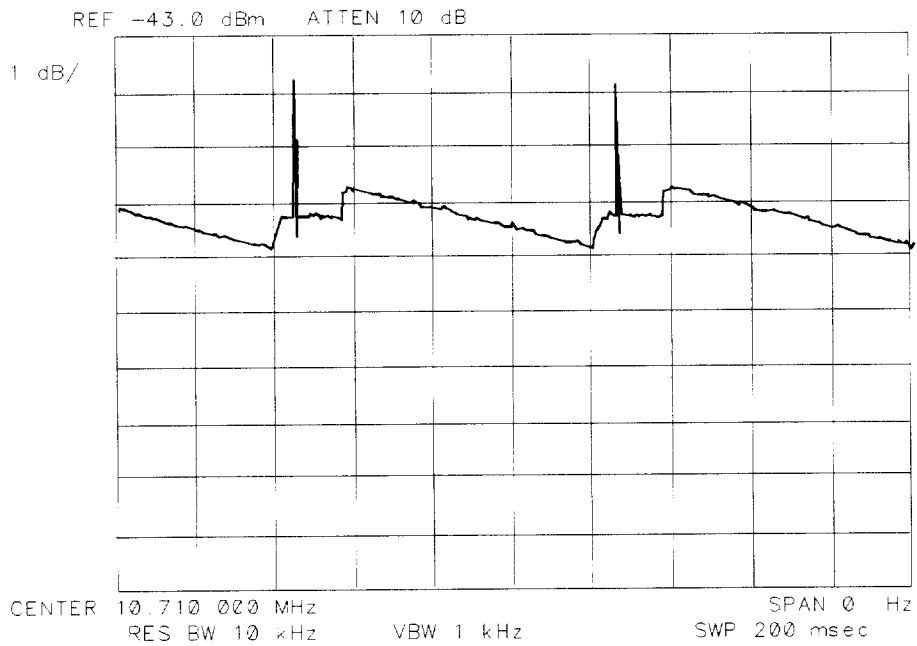


Figure 8-20. Failed Crystal Set Symptoms

SK 189

## Low-Pass Filter

Refer to function block AB of A4 Log Amplifier Schematic Diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

1. Connect a DVM positive probe to A4J9 pin 4.
2. On the spectrum analyzer, press **CAL**.
3. Press **FULL IF ADJUST**. Observe the DVM reading between the displayed messages **IF ADJUST STATUS: 300 kHz RBW** and **IF ADJUST STATUS: 3 kHz RBW**. During this time period, the voltage should be within a 2 to 10 Vdc range.
4. Observe the DVM reading while **IF ADJUST STATUS: AMPLITUDE** is displayed. The reading should be within the 2 to 10 Vdc range.
5. If the DVM reading is outside the range in step 3 but inside the range in step 4, suspect one of the filter's reactive components.

## Sweep Generator

Refer to function block Z of A4 log amplifier schematic diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

A properly operating sweep generator generates a series of negative-going parabolas. Before the sweep, switches A4U802C and A4U802D turn on, shorting A4C802 and A4C801 (the output is at 0 volts). These switches open to start the sweep. The output of A4U804A, pin 1, is 0.35 V to 10 V, depending on the sweep width selected by A4U802A and A4U803A. This voltage appears across A4R801. Capacitor A4C801 integrates the current through A4R801. The output of A4U804B is a straight, negative-going ramp. Capacitor A4C802 and resistor A4R802 integrate the output of A4U804A which starts a negative ramp (A4U804C) at the beginning of the sweep. The ramp from A4U804B is added to the current in A4R802 via A4U803B. Integrating this ramp results in the parabolic output waveform.

## AM/FM Demodulation, Audio Amplifier, and Speaker

Refer to function blocks R, S, and T of A4 Log Amplifier Schematic (sheet 4 of 4) Diagram in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

If the audio circuits are not functioning use the following procedure to isolate the problem.

1. Set an AM signal generator controls as follows:

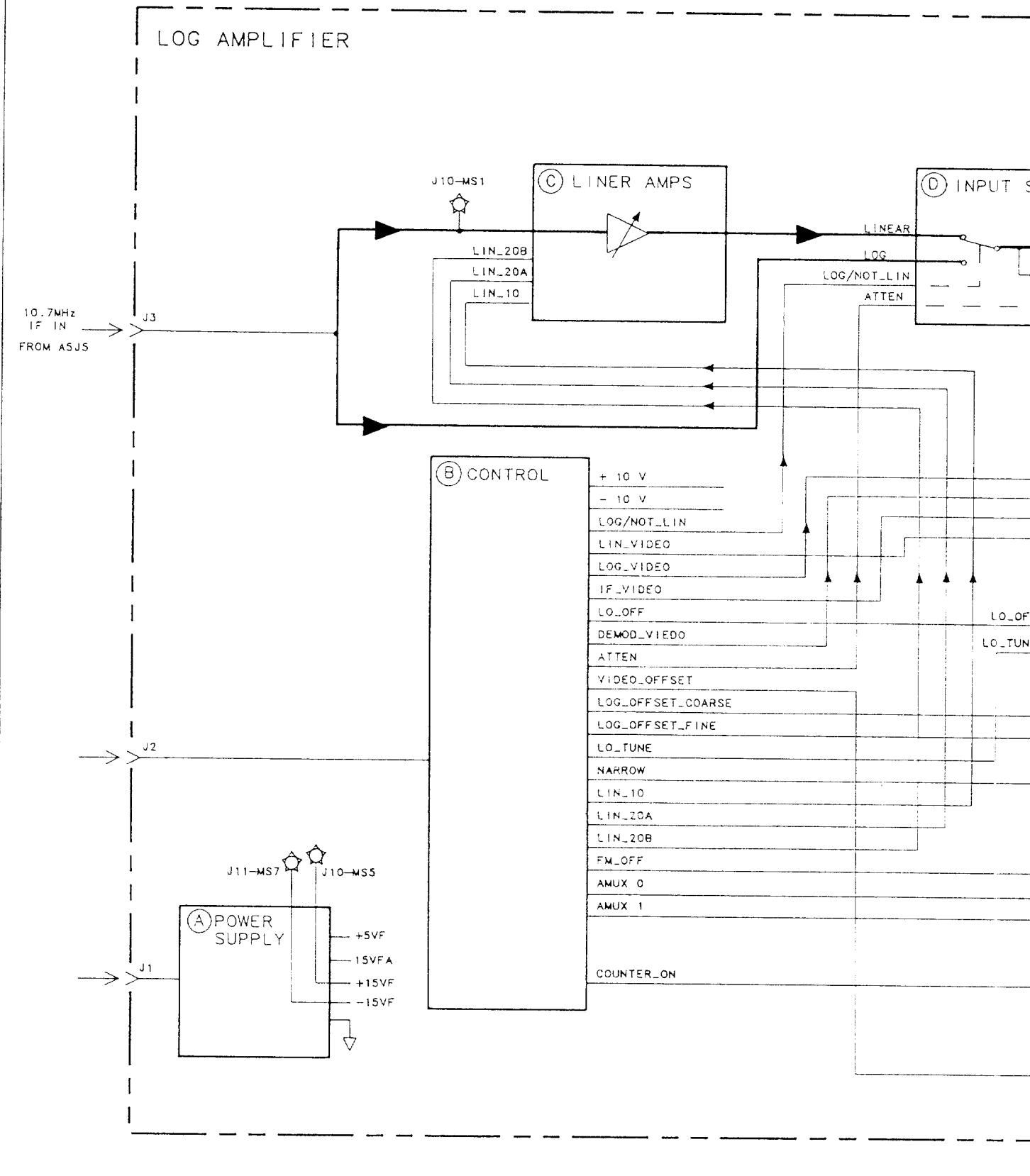
|                            |         |
|----------------------------|---------|
| Frequency .....            | 100 MHz |
| Amplitude .....            | -6 dBm  |
| Modulation type .....      | 80% AM  |
| Modulation frequency ..... | 400 Hz  |

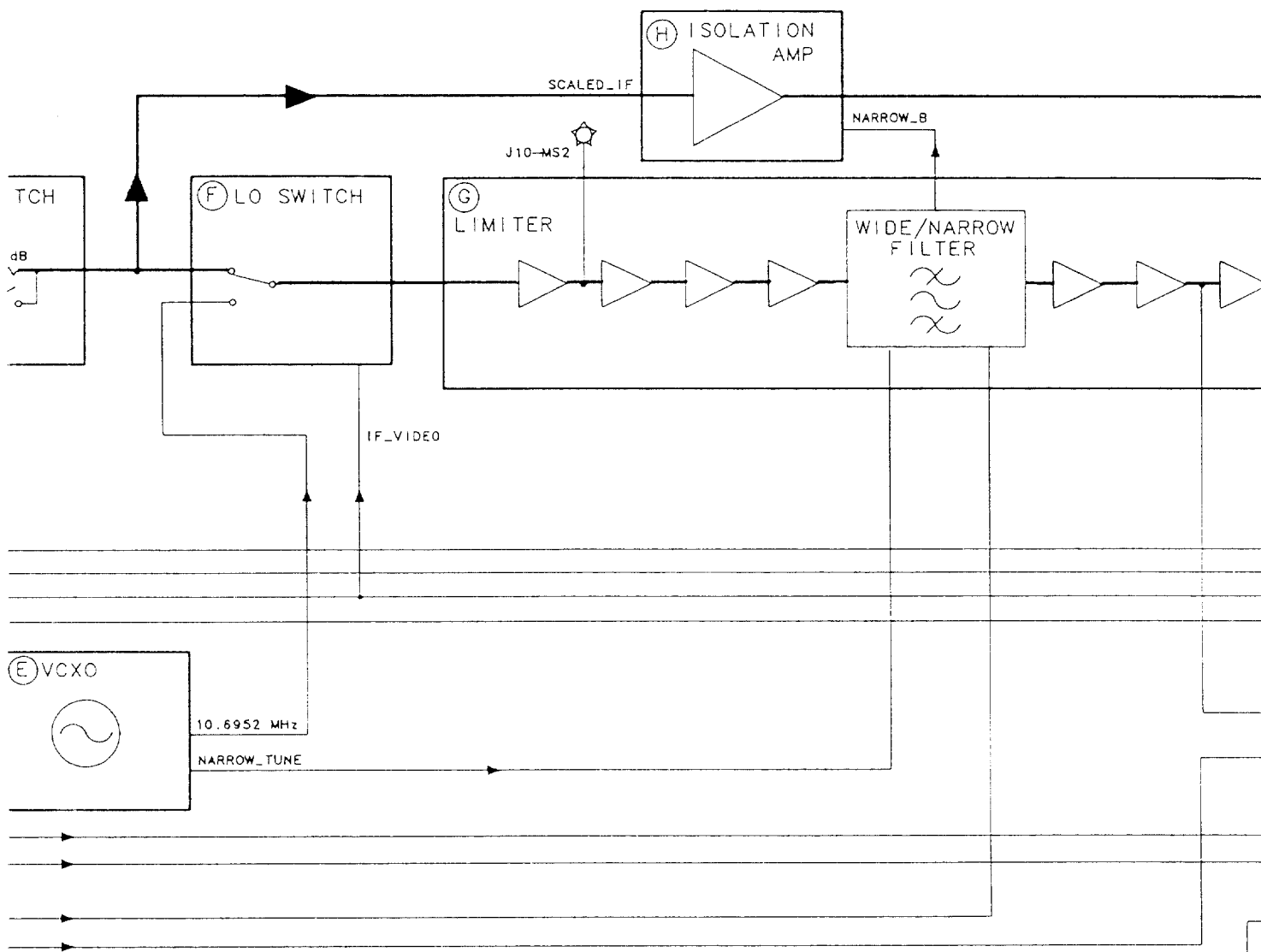
2. Set the spectrum analyzer controls as follows:

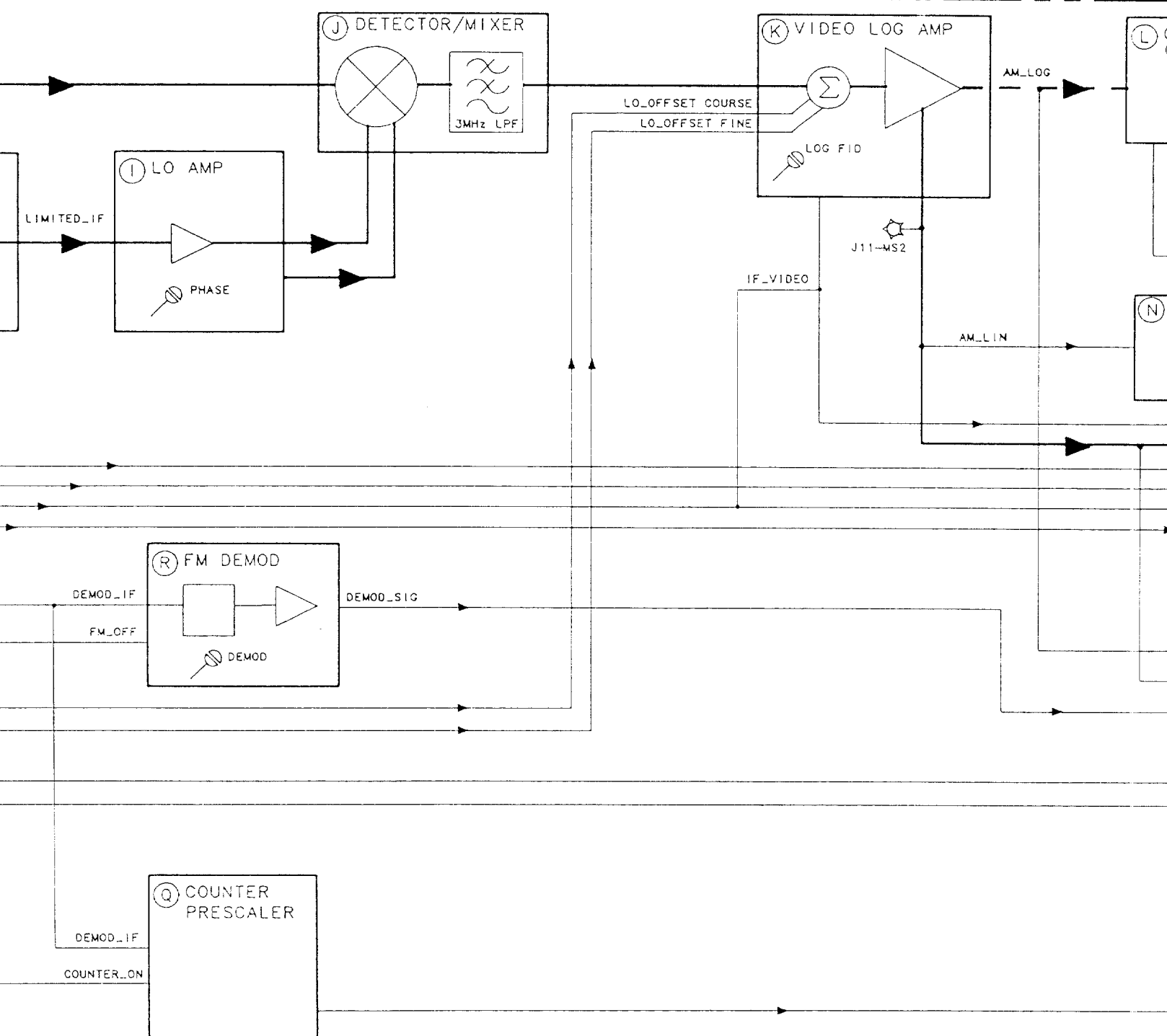
|                            |         |
|----------------------------|---------|
| Center frequency .....     | 100 MHz |
| Span .....                 | 0 Hz    |
| Sweep time .....           | 50 ms   |
| Reference level .....      | 0 dBm   |
| Resolution bandwidth ..... | 10 kHz  |
| Amplitude scale .....      | LINEAR  |

3. Adjust the spectrum analyzer reference level and center frequency to display the 400 Hz modulation frequency eight divisions peak-to-peak.
4. On the spectrum analyzer, press **AUX CTRL**, **AM/FM DEMOD**, **AM DEMOD ON**, and set the sweep time to 5 seconds.
5. Vary the volume and listen for the variation in speaker output level. Clipping is normal at the highest volume levels.
6. If the audio is not working correctly monitor the signal at A4U704 pin 3 with an oscilloscope. The signal should be 20 mV peak-to-peak  $\pm 25\%$  (with +2.5 V of dc bias). If the signal measures outside these limits, the fault is prior to the audio amplifier (block T).
7. If the signal is correct, troubleshoot the audio amplifier and speaker.

# A4 LOG AMPLIFIER/CAL OSCILLATOR BLOCK DIAGRAM







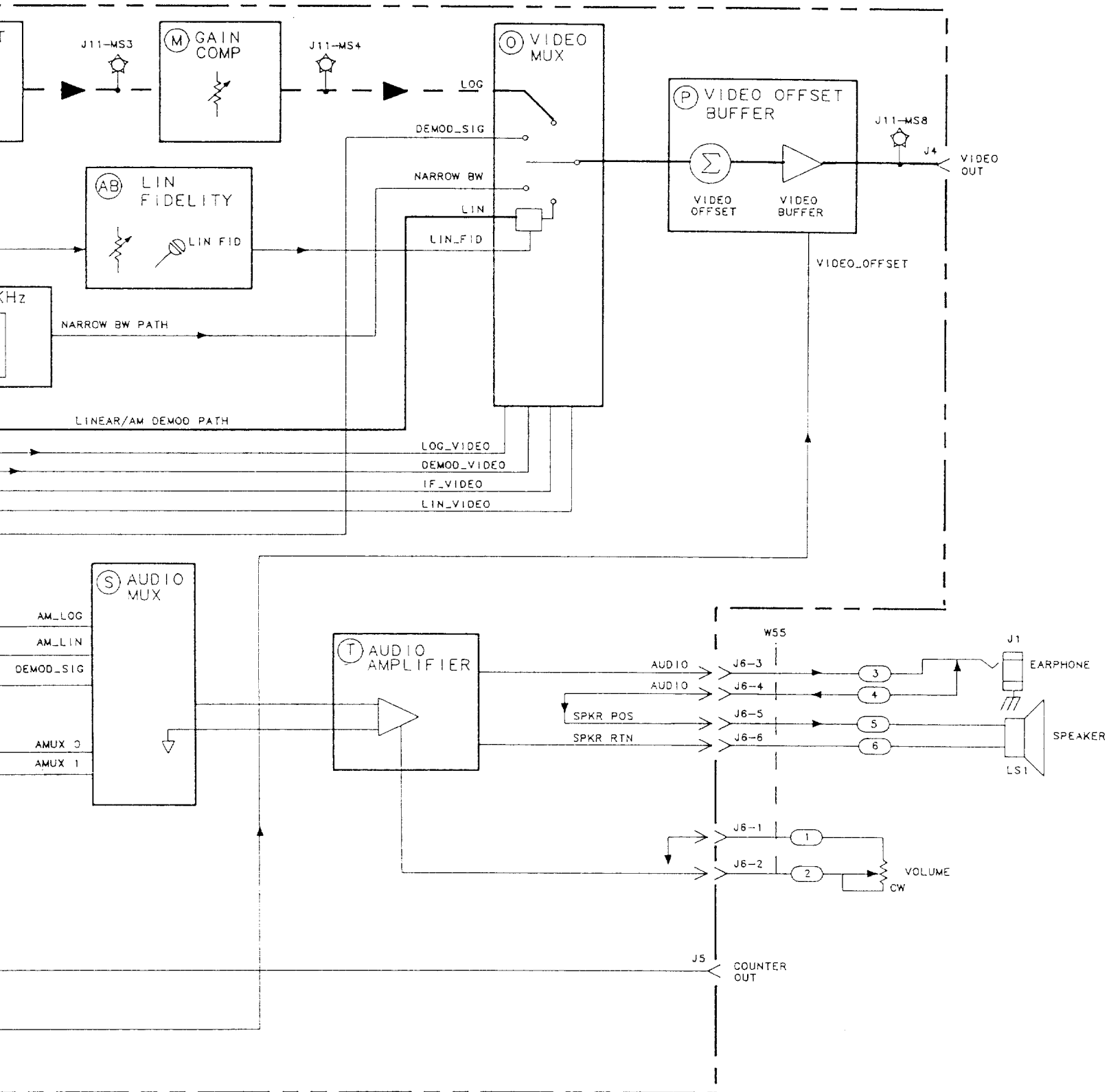
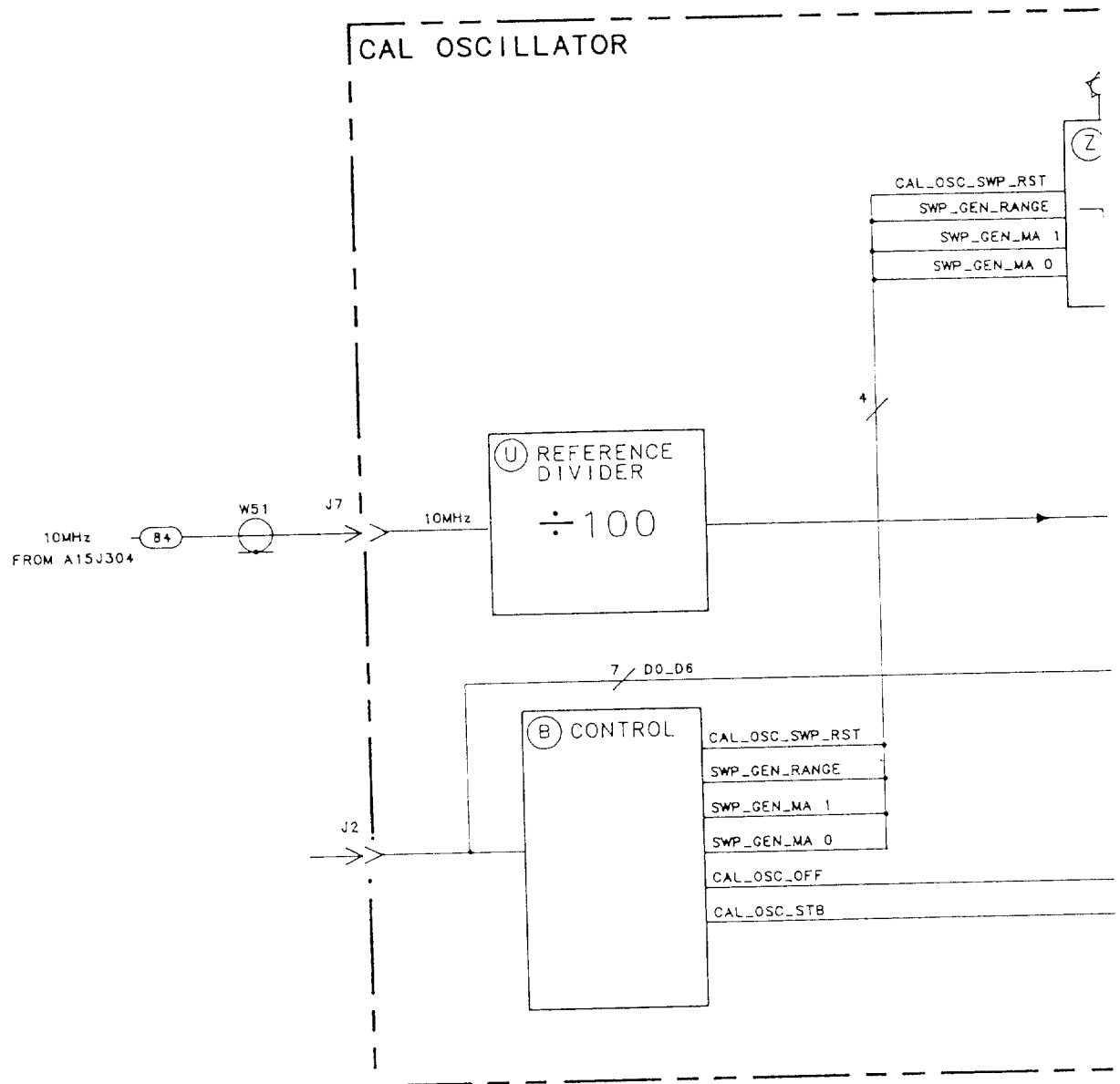
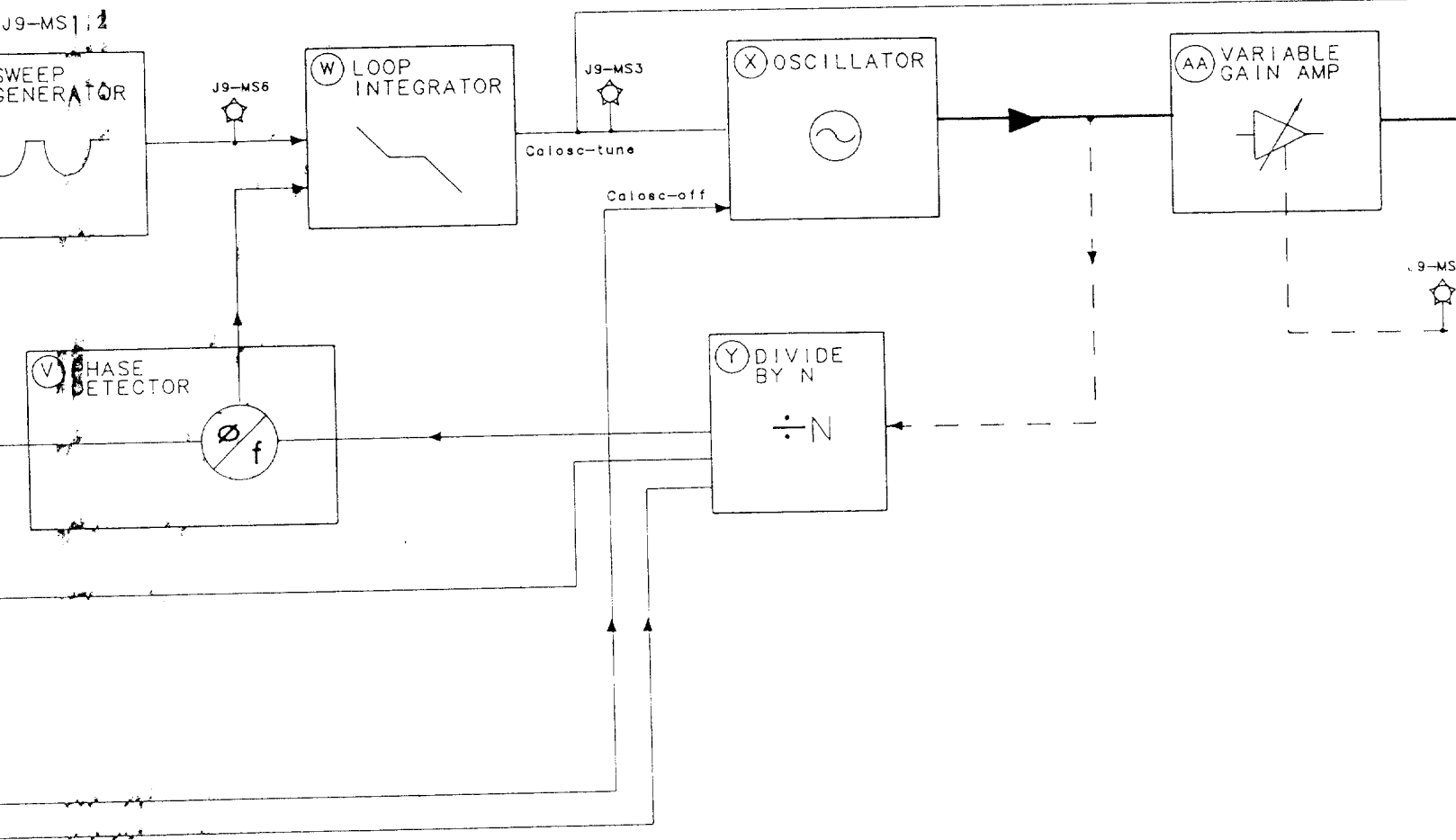


FIGURE 8-21. A4 LOG AMPLIFIER/CAL OSCILLATOR BLOCK DIAGRAM (1 of 2)

A4 LOG AMPLIFIER/CAL OSCILLATOR BLOCK DIAGRAM





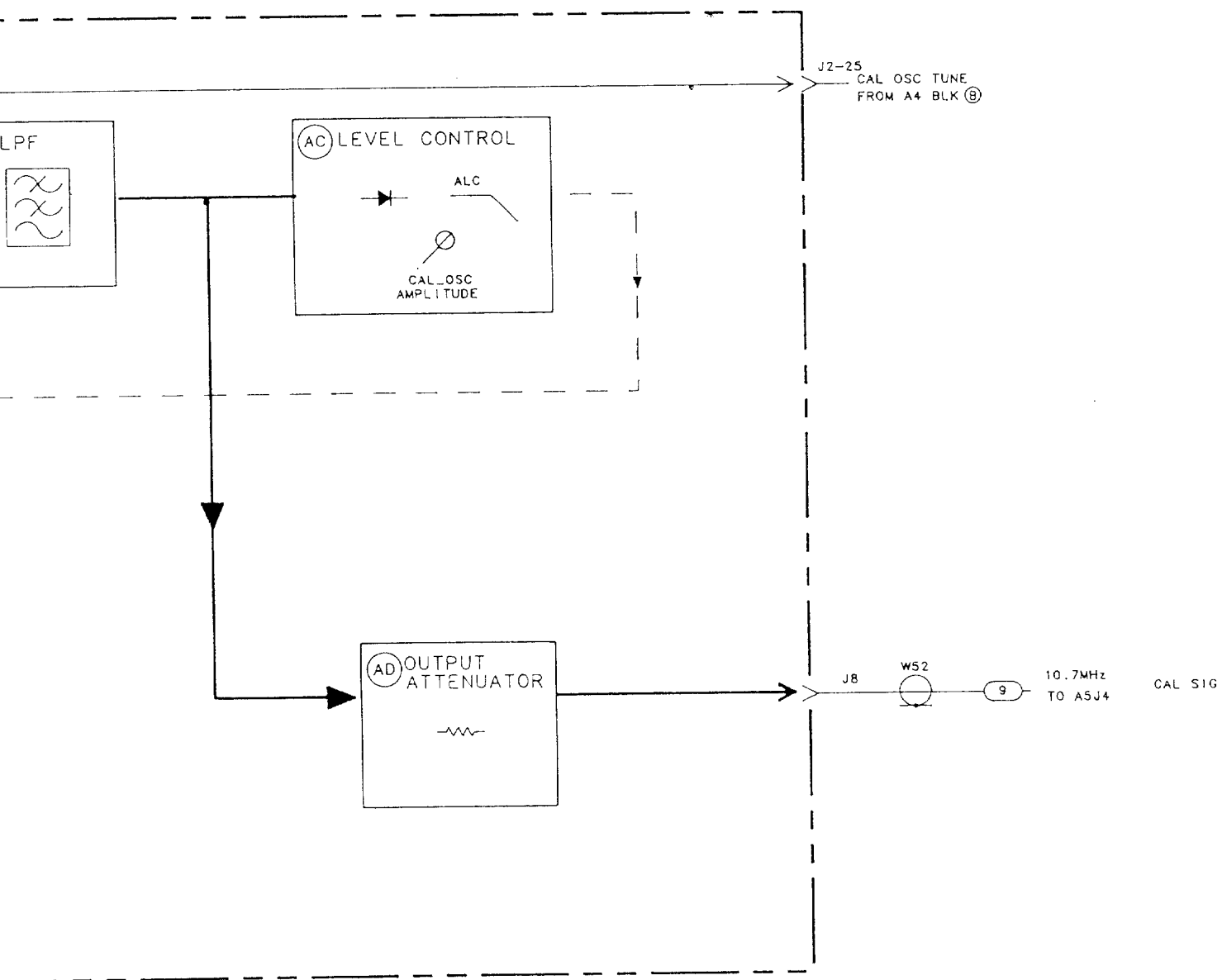
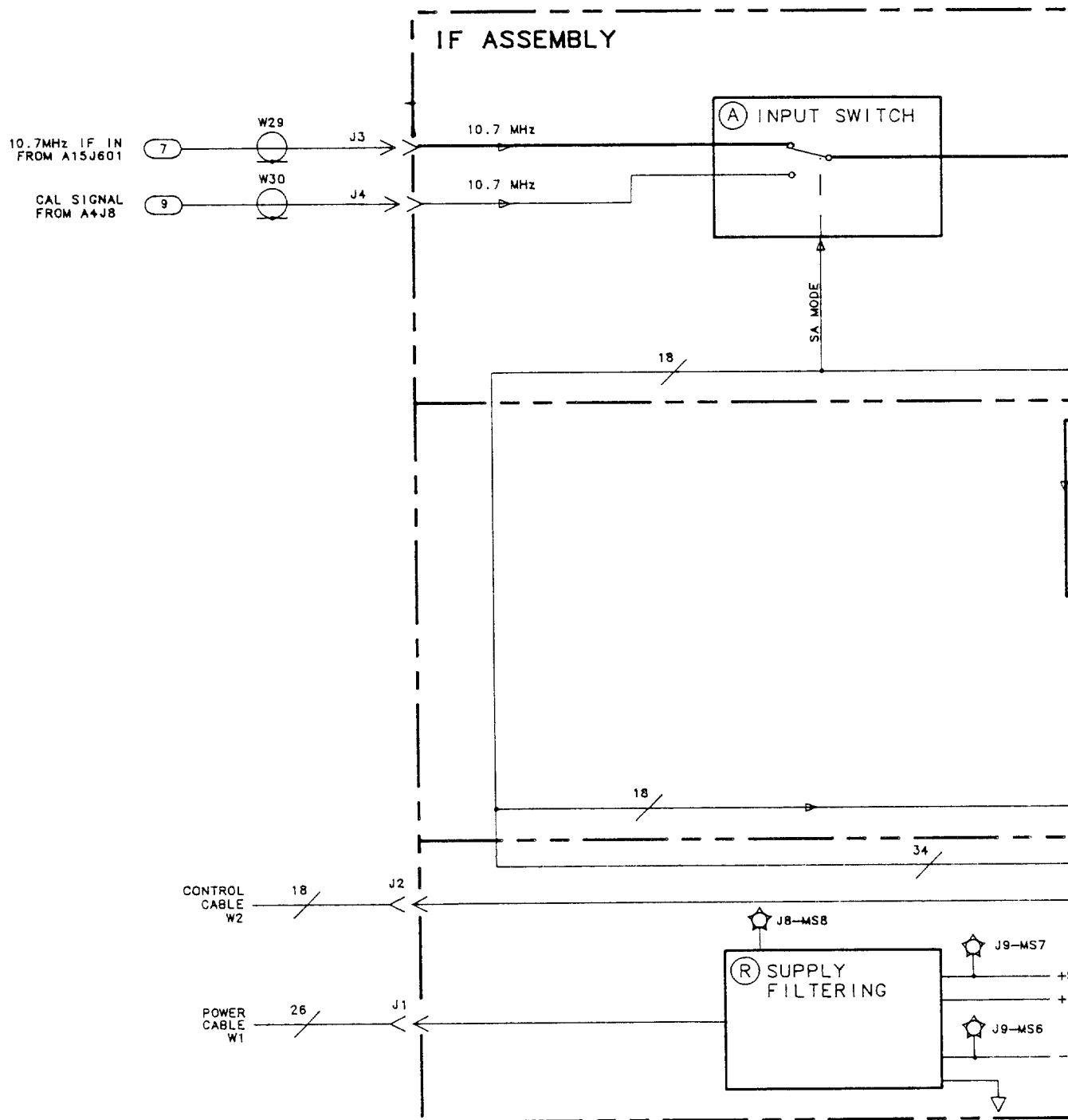
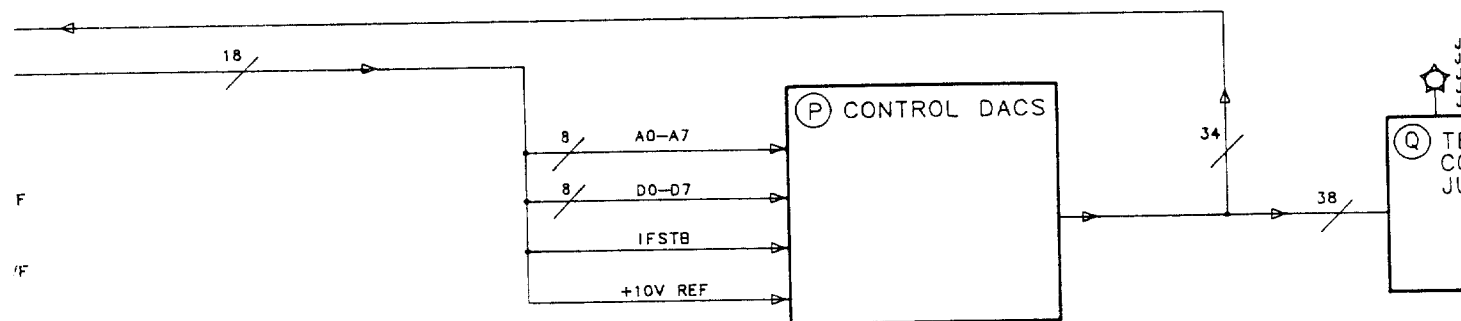
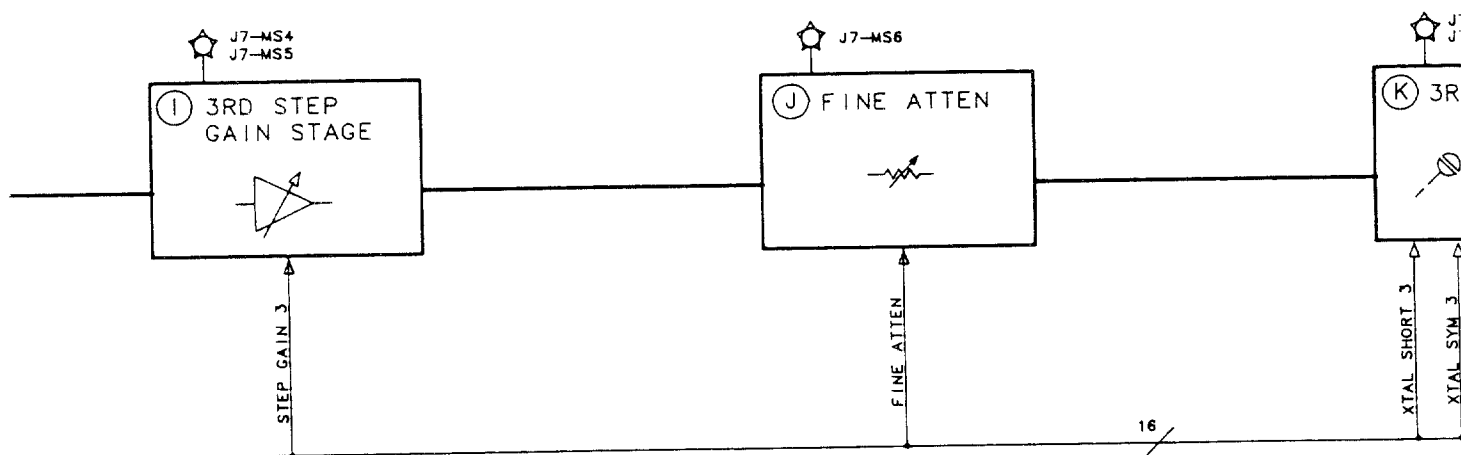
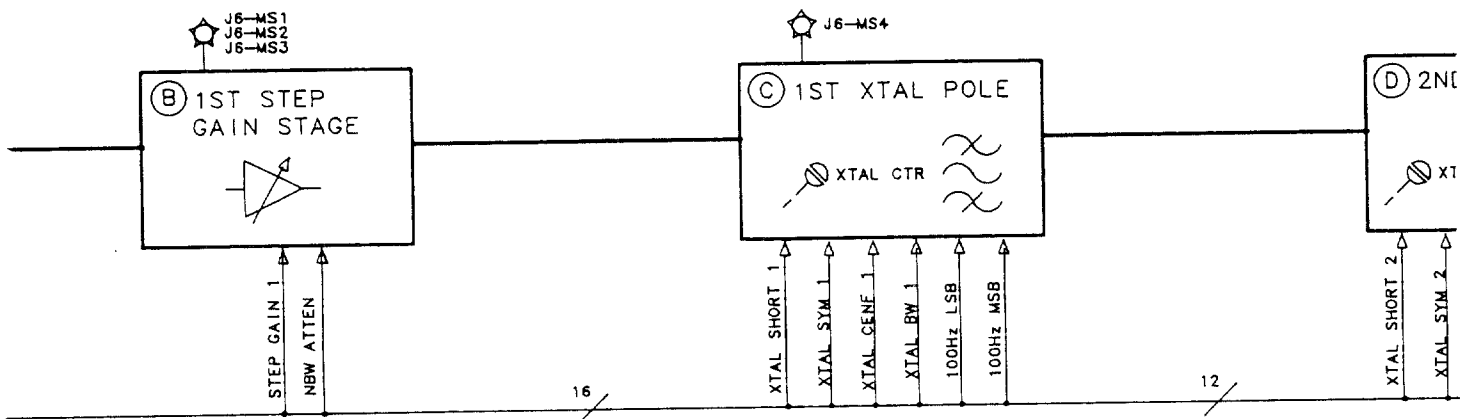
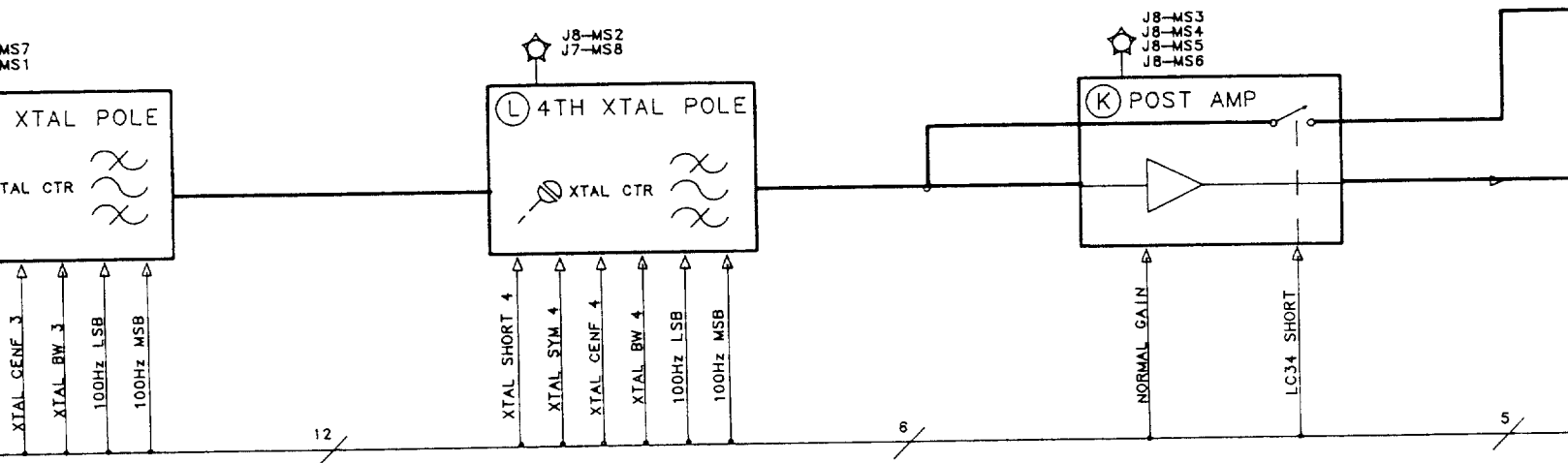
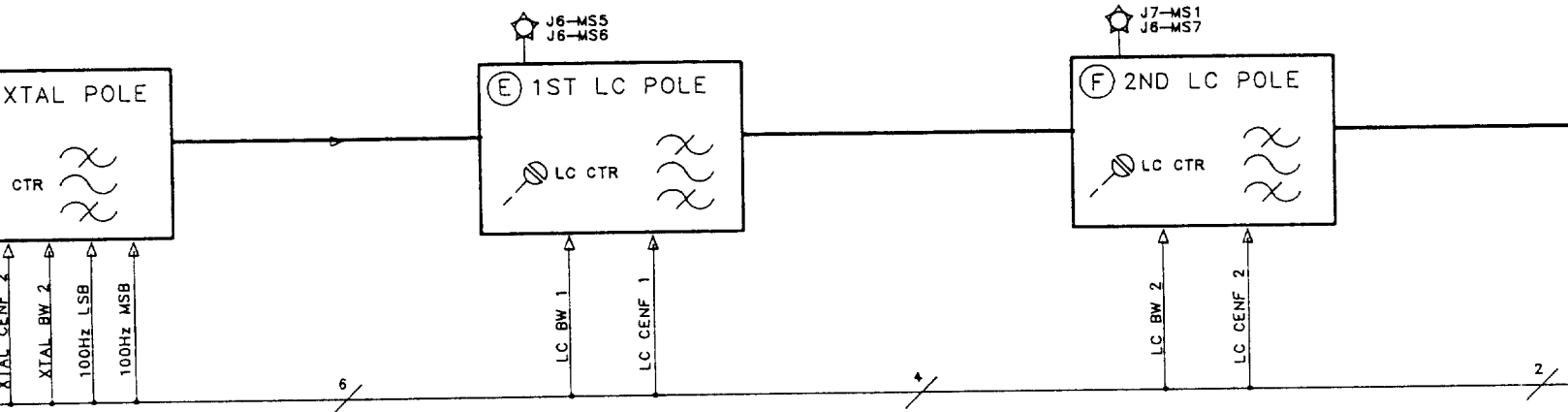


FIGURE 8-21. A4 LOG AMPLIFIER/CAL OSCILLATOR BLOCK DIAGRAM (2 of

# A5 IF ASSEMBLY BLOCK DIAGRAM







MS1  
MS2  
MS3  
MS4  
MS5

ST  
NNECTOR  
UNCTION

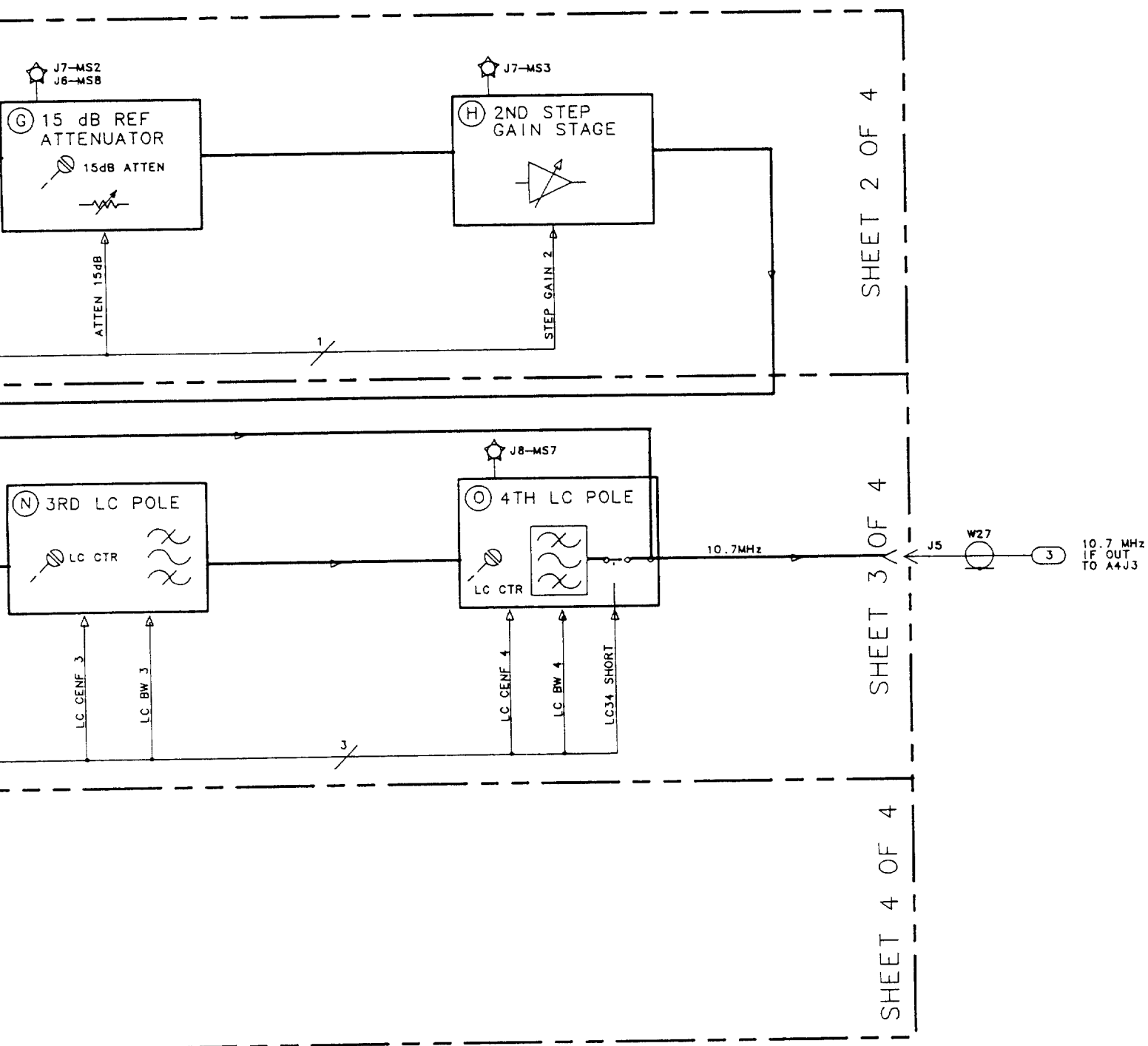


FIGURE 8-22. A5 IF ASSEMBLY BLOCK DIAGRAM

## Controller Section

---

The controller section includes the A2 controller assembly, A19 HP-IB assembly, and BT1 battery. The presence of a display (graticule and annotation) verifies that most of A2 controller assembly is operating properly.

- Troubleshooting Using the TAM
  - Blank Display
  - Digital Signature Analysis (DSA)
  - Display Problems
    - Line Generators
    - Blanking
    - Display Jumbled or Trace Off Screen
    - Intensity
    - Bad Characters or Graticule
    - Long Lines Dimmer than Short Lines
  - Analog Zero-Span Problems
  - Frequency-Count Marker Problems
  - Frequency Counter
  - State- and Trace-Storage Problems
  - Keyboard Problems

**Note**

When measuring voltages or waveforms, make ground connections to A2TP3. The metal board-standoffs are not grounded and should not be used when taking measurements.

## Troubleshooting Using the TAM

Table 9-1 lists assembly test connectors associated with each Manual Probe Troubleshooting test. Figure 9-1 illustrates the location of A2's test connectors.

**Table 9-1. TAM Tests versus Test Connectors**

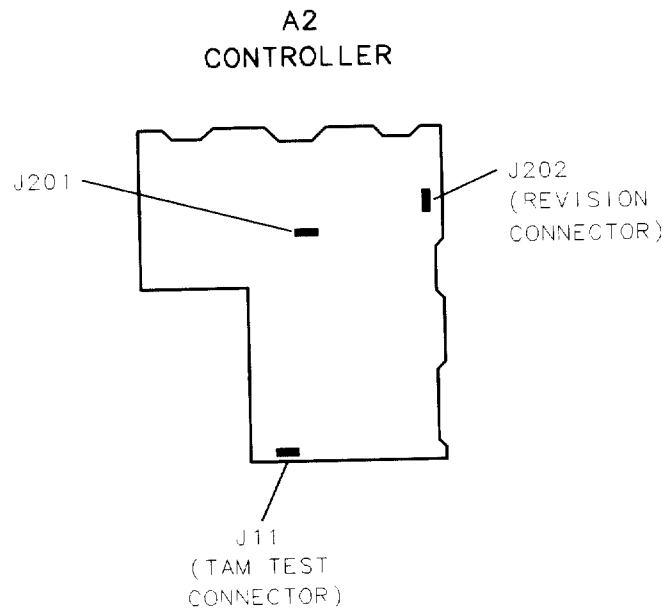
| Connector | Manual Probe Troubleshooting Test                                                                                                          | Measured Signal Lines                            |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------|
| A2J11     | ADC/MUX Test<br>DAC test                                                                                                                   | MS1, MS3 through MS6, MS8<br>MS2, MS7, OS1       |
| A2J201    | 10 volt reference test<br>Switch drive test<br>Buffered X & Y DAC outputs<br>X line gen test<br>Y line gen test<br>Intensity offset output | MS4<br>MS8<br>MS2, MS7<br>MS6<br>MS1<br>MS3      |
| A2J202    | Revision<br>X, Y, & Z Output Offset<br>X output amplifier<br>Y output amplifier<br>Blanking test<br>Focus DAC test                         | MS1<br>MS3, MS4, MS7<br>MS7<br>MS3<br>MS8<br>MS2 |

### Blank Display

Use the following procedure if the instrument's display is blank. This procedure substitutes an HP-IB printer for the display.

1. Connect the printer to the HP 8560E and set the printer's address to the value required by the TAM. This is usually 1.
2. All of the power-supply indicator LEDs along the edge of the A2 controller assembly should be lit.
3. The rear-panel CRT +110 VDC ON indicator might not be lit, even if the +110 V is present.
4. Connect the TAM's probe cable to A2J11.
5. Press **MODULE**, **SOFT KEY #3**, **⇓**, and **SOFT KEY #1**. (The top soft key is #1.)
6. The yellow LED next to A2J11 should blink approximately ten times. If the LED fails to blink correctly, troubleshoot the digital section of the A2 controller assembly.
7. Move the probe cable to A2J202. Press **SOFT KEY #1** and wait five seconds.

8. Press **SOFT KEY #4**. The results should be sent to the printer.
9. If a failure is indicated in any of these tests, the fault lies on the A2 controller assembly.  
To obtain more information:
  - a. Press the step down key,  one less time than the test number. (For example, press it twice for the third test on the list.)
  - b. Press **SOFT KEY #3**, then **SOFT KEY #4**, and when the printout is complete, **SOFT KEY #6**.



SP17

**Figure 9-1. A2 Test Connectors**

10. Move the probe cable to A2J201, press **SOFT KEY #1** and wait five seconds.
11. Press **SOFT KEY #4**. The results will be sent to the printer. Follow the procedure in step 9 to obtain more information on any of the tests.
12. If no failures were indicated in testing the A2 controller, move the probe cable to A17J4.
13. Press **SOFT KEY #1** and wait five seconds.
14. Press **SOFT KEY #4**. The results will be sent to the printer.
15. If no failure is indicated in the printout, refer to "High Voltage Supplies" in Chapter 12.

---

## Digital Signature Analysis (DSA)

Digital signature analysis (DSA) places microprocessor, A2U1, in a simplified known state. This simplified state consists of placing a one-word instruction, MOVE QUICK, (0111 XX10 XXXX XXX0) on the data bus. The microprocessor cycles through its address range continually reading the instruction. Perform the following DSA procedure to test the operation of microprocessor, A2U1:

1. Set the HP 8560E's **LINE** switch off.
2. Move the DSA jumper on J3 (located in the middle of the A2 assembly) from the DISable position to the ENable position.
3. Remove jumper A2E1. A2E1 is a 16 pin dual-in-line package located in the middle of the A2 Assembly. Set the HP 8560E's **LINE** switch on.
4. Use an oscilloscope to confirm that address lines, address strobe, and chip selects are toggling at proper levels.
5. Use an oscilloscope to check the address line sequencing. The signal on each line (starting with A1 and ending with A23) should be one-half the frequency of the previous line.
6. If step 4 reveals problems, microprocessor A2U1 is probably faulty.
7. Set the HP 8560E's **LINE** switch off. Replace jumper A2E1. Move the DSA jumper from connecting E5 and E6 back to connecting E6 and E7.

---

## Display Problems

### Line Generators

Refer to function blocks D and I of A2 controller schematic diagram (sheet 1 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The line generators convert the digital display information to an analog output suitable to drive the A17 CRT driver assembly. These circuits change the digital words into vectors, or lines, which move the beam of the CRT. The vectors are each 6  $\mu$ s long (width of the INTEGRATE pulse) followed by a 1  $\mu$ s SAMPLE pulse. When characters of text are being drawn, the vectors are 3  $\mu$ s long.

1. On the HP 8560E press **PRESET**.
2. On the HP 8560E, press **CAL**, **MORE**, and **CRT ADJ PATTERN**. If the display is blank, press the bottom softkey and then the top softkey.
3. Set an oscilloscope to the following settings:

|                 |                |
|-----------------|----------------|
| Amplitude scale | ..... 3 V/div  |
| Sweep time      | ..... 1 ms/div |
| Triggering      | ..... External |
4. Externally trigger the oscilloscope off the signal at A2U207 pin 8 (LBRIGHT).

5. Compare the signals at the following test points with those illustrated in Figure 9-2.

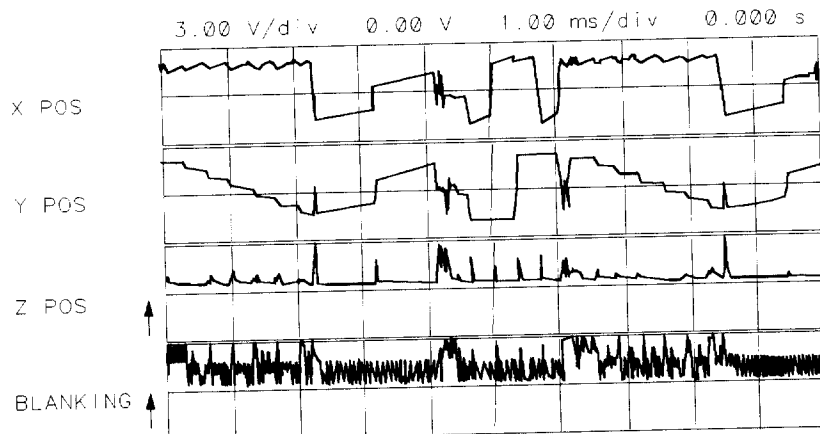
X POS: A2J202 pin 14  
 Y POS: A2J202 pin 3  
 Z OUT: A2J201 pin 3  
 BLANKING: A2J202 pin 15

---

**Note** Waveforms displayed on an analog scope may show considerably more spikes. This is normal and is due to the wider displayed bandwidth.

---

6. Troubleshoot the circuits associated with any bad waveforms.



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**Figure 9-2. Line Generator Output Waveforms**

## Blanking

Refer to function block J of A2 Controller Schematic Diagram (sheet 1 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

- Using an oscilloscope, check for blanking pulses at A2J202 pin 15. A2U206 pin 6 should be at a TTL high. Blanking pulses turn the CRT beam off during the sample time of the line generators and when moving the CRT beam to a new position for drawing the next vector.
- Set an oscilloscope to the following settings:
 

|                  |       |                |
|------------------|-------|----------------|
| Amplitude scale  | ..... | 4 V/div        |
| Amplitude offset | ..... | +2.5 V         |
| Sweep time       | ..... | 20 $\mu$ s/div |
| Triggering       | ..... | External       |
- Externally trigger the oscilloscope off the signal at A2U207 pin 8 (LBRIGHT).

4. Compare the blanking-circuit input signals at the following test points with those illustrated in Figure 9-3.

BLANKING: J202 pin 15

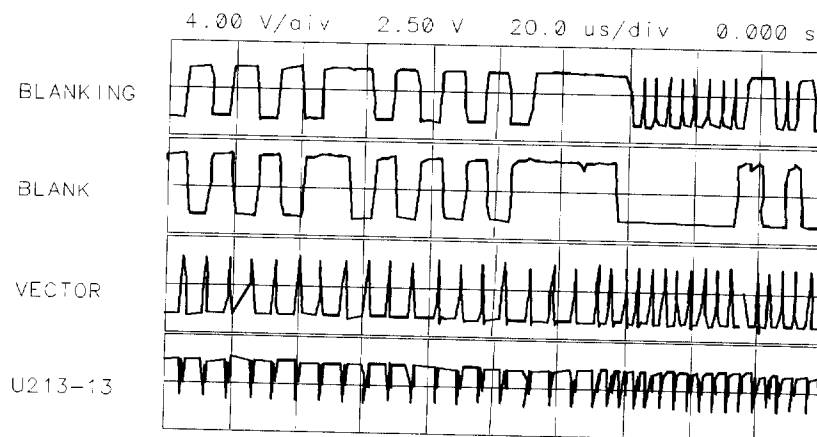
BLANK: U214 pin 12

VECTOR: U214 pin 11

U213 pin 13

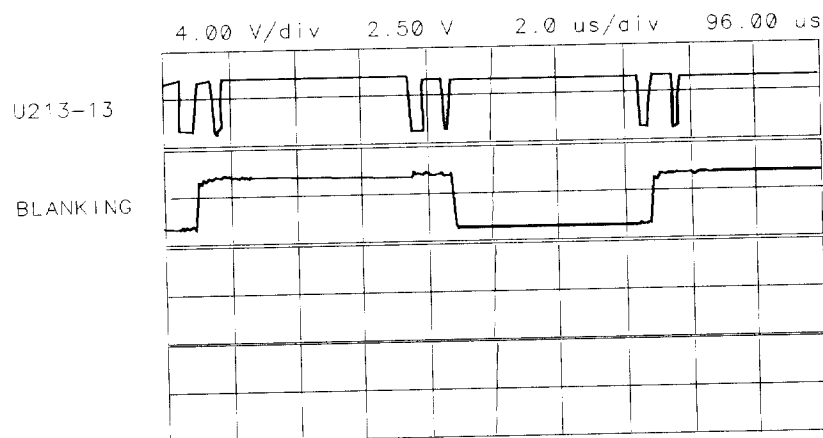
5. The waveforms in Figure 9-3 must match the timing of the vectors being drawn. To do this, U215B is used to adjust the leading edge, and U215A is used to adjust the trailing edge. The first six horizontal divisions show the line drawing mode where the VECTOR pulses are  $6\ \mu\text{s}$  apart. The remaining divisions shows character mode (VECTOR pulses  $3\ \mu\text{s}$  apart). The BLANK pulses are synchronized to the VECTOR pulses by U214B. The fourth trace shows the double pulses which delay the leading and trailing edges of the blanking pulses.
6. Set the oscilloscope to the following settings to expand the first and fourth traces. This displays how the rising edges of U213-13 determine the transitions of the blanking pulses. See Figure 9-4.

Amplitude scale ..... 4 V/div  
 Amplitude offset ..... +2.5 V  
 Sweep time .....  $2\ \mu\text{s}/\text{div}$   
 Delay from trigger .....  $96\ \mu\text{s}$   
 Triggering ..... External



SK192

**Figure 9-3. Blanking Waveforms**



SK193

**Figure 9-4. Expanded Blanking Waveforms**

### Display Jumbled or Trace Off Screen

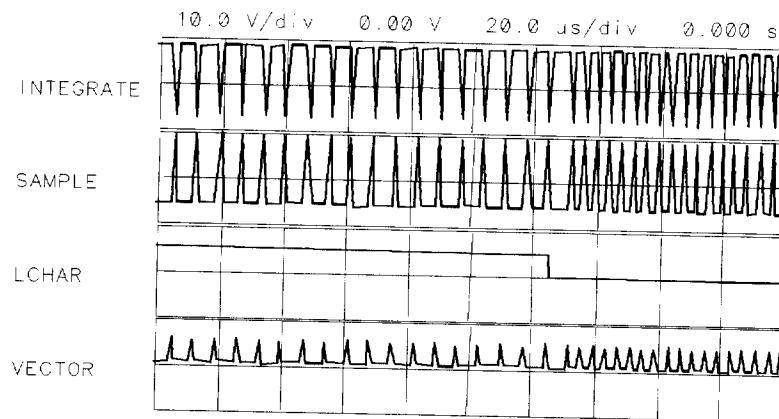
Refer to function blocks D and I of A2 controller schematic diagram (sheet 1 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The two line generators are identical circuits, so the following steps apply to both. The X generator is referenced below, with Y generator references in parentheses.

1. The voltage at A2U202B pin 7 should measure 10.0 V.
2. Perform steps 1 through 5 of "Line Generators" in this chapter. If the X POS and Y POS waveforms look different from those illustrated in Figure 9-2, check the waveforms at the low-pass filter's input (function block E in the component-level information binder).
3. The waveform at the low-pass filter should look like X POS in Figure 9-2 but have an amplitude from 0 V to +5 V.
4. If the waveform in step 3 is incorrect, set an oscilloscope to the following settings:
 

|                 |       |                |
|-----------------|-------|----------------|
| Amplitude scale | ..... | 10 V/div       |
| Sweep time      | ..... | 20 $\mu$ s/div |
| Triggering      | ..... | External       |
5. Trigger the oscilloscope on the signal at U207 pin 8 (LBRIGHT).
6. Compare the line-generator input signals at the following test points with those illustrated in Figure 9-5. INTEGRATE and SAMPLE waveforms are replicas of VECTOR except for polarity and amplitude. LCHAR is low when characters are drawn.

|            |                  |
|------------|------------------|
| INTEGRATE: | Q202's collector |
| SAMPLE:    | Q201's collector |
| LCHAR:     | U207 pin 9       |
| VECTOR:    | U213 Pin 9       |



SK194

**Figure 9-5. Switch Driver Waveform LCHAR**

7. All of the DAC inputs should change state two or more times within a 5 ms window. If one or more DAC bits are not working correctly, this will effect the entire display, especially the diagonal lines that go from lower left to upper right. When these lines are drawn, both the X and Y DACs are stepped one count at a time. A “stuck” bit will distort the diagonal in a repetitive manner. The quicker the repetition, the less significant the “stuck” bit. Horizontal distortions apply to the X LINE GENERATOR DAC, while vertical distortions apply to the Y LINE GENERATOR DAC. The DACs have current outputs so they are not readily observable with an oscilloscope. Continue with step 8 to observe the DAC outputs.
8. To break the effect of feedback in the line generators and to observe the output of the DACs, short J201 pin 13 (J201 pin 1) to TP3 (GND) to observe U201 pin 1 and TP2 (U203 pin 1 and TP1.) Continue with step 9.
9. Set an oscilloscope to the following settings:
 

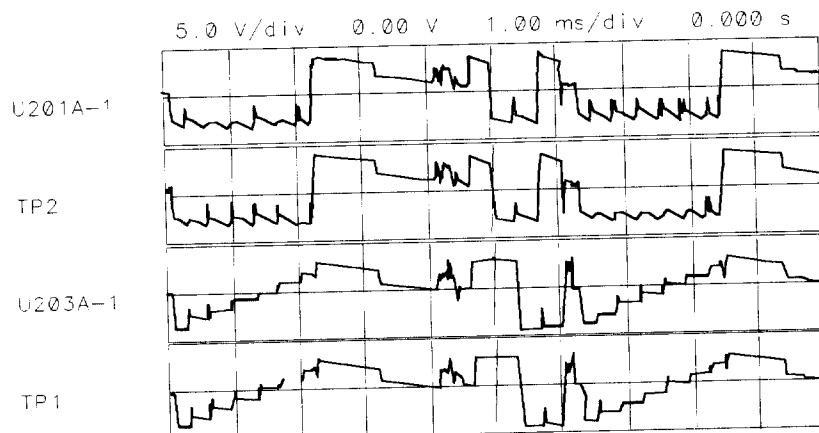
|                 |                |
|-----------------|----------------|
| Amplitude scale | .....5 V/div   |
| Sweep time      | .....1 ms/div  |
| Coupling        | .....ac        |
| Triggering      | ..... External |
10. Trigger the oscilloscope on the signal at U207 pin 8 (LBRIGHT).
11. The following waveforms should look like Figure 9-6 on the oscilloscope. The top two traces are for the X line generator and the bottom two traces for the Y line generator.
 

|                  |  |
|------------------|--|
| X line generator |  |
| U201 pin 1       |  |
| TP2              |  |
| Y line generator |  |
| U203 pin 1       |  |
| TP1              |  |

12. Figure 9-7 illustrates the waveforms in step 11 expanded to show relative timing. the second and fourth traces are delayed by 5 ms from the first and third. The oscilloscope settings are changed as follows:

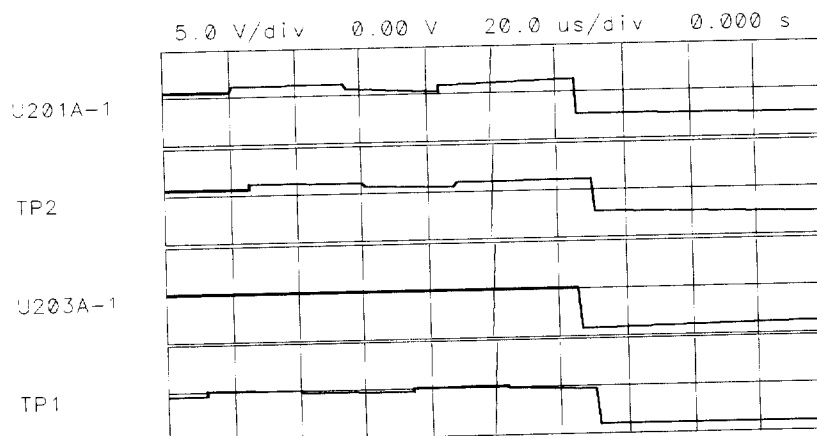
Sweep time ..... 20  $\mu$ s/div

13. Figure 9-8 illustrates the waveforms of properly working line generators. Whenever there is a pulse on TP2 (or TP1), the appropriate integrator U201B (or U203B) generates a ramp (the output vector) which feeds back to U201A (U203A) and shows on its output.



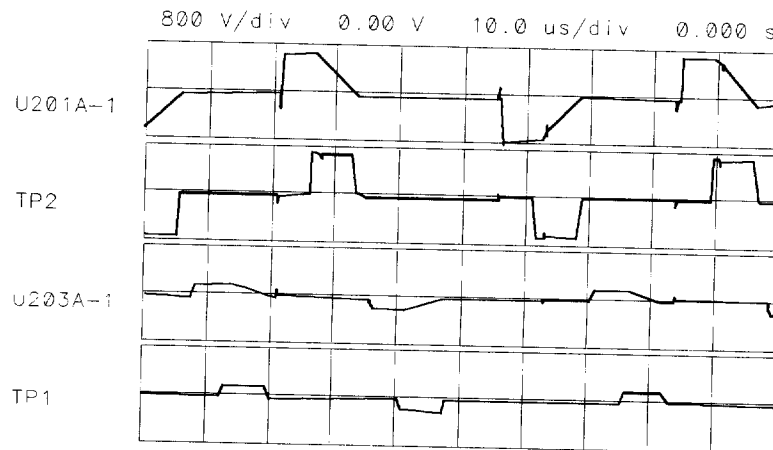
SK195

**Figure 9-6. Distorted X/Y Line Generator Waveforms**



SK196

**Figure 9-7. Expanded X/Y Line Generator Waveforms**



SK197

**Figure 9-8. Normal X/Y Line Generator Waveforms**

### Intensity

1. The length of the vector being drawn can effect intensity. U210A, U210C, and U210D sum the lengths of the X and Y vectors. Refer to “Long Lines Dimmer than Short Lines” in this chapter.
2. Short A2U207 pin 6 to pin 7. If the display does not brighten, troubleshoot LBRIGHT switch, U207B. This switch intensifies trace A and active softkeys.
3. Short A2U207 pin 2 to pin 3. If the display does not brighten, troubleshoot DEF1 switch, U207A. This switch is used in analog zero-span.
4. Change the intensity (under **DISPLAY**). If the intensity does not change, troubleshoot the intensity DAC, A2U212A. (A2U212A is controlled from the front panel.) The amplitude of the waveform at U211A pin 1 should increase or decrease with intensity changes.
5. Clamp U211B limits the voltage to about 4.2 V. Short A2J201-1 to ground and set the intensity DAC to a number greater than 80. A major portion of the waveform should be limited to 4.2 V.
6. If a major portion of the waveform is not limited to 4.2 V, troubleshoot the maximum brightness clamp, A2U211C.

### Bad Characters or Graticule

If the displayed characters are bad but the graticule is correct (or if the symptoms are reversed), troubleshoot the X- and Y- generator switches A2U207D and A2U207C. Check that the switch driver signal LCHAR is working properly. Refer to “Display Jumbled or Trace Off Screen” in this chapter.

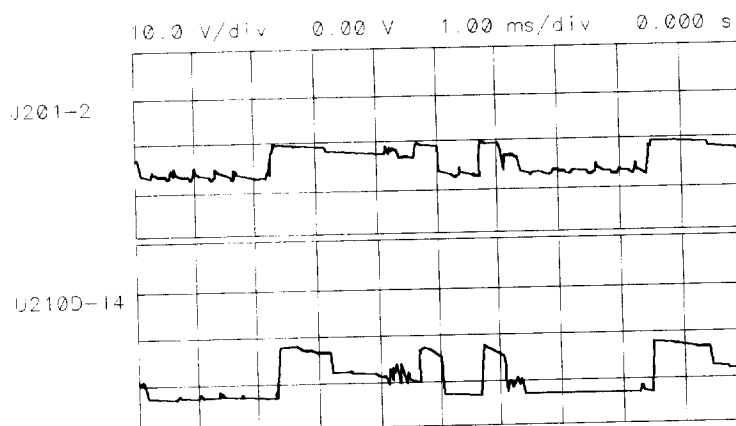
## Long Lines Dimmer than Short Lines

Refer to function block M of A2 controller schematic diagram (sheet 1 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The Z output function block contains the absolute value circuits which determine the intensity of vectors drawn on the display. The vector length is approximated by the sum of the X length and Y length. The voltage corresponding to the X length,  $\Delta X$ , is converted to current by R274. If the voltage is negative, it is amplified by 2 in A2U210C, converted to current by A2R246, and added to the current from A2R274. This effectively turns both negative and positive voltages into positive currents, hence absolute value.

1. Short A2J201 pin 13 to ground (A2TP3).
2. Connect channel A of an oscilloscope to A2J201 pin 2. Connect channel B to A2U210D-14.
3. Set an oscilloscope to the following settings:
 

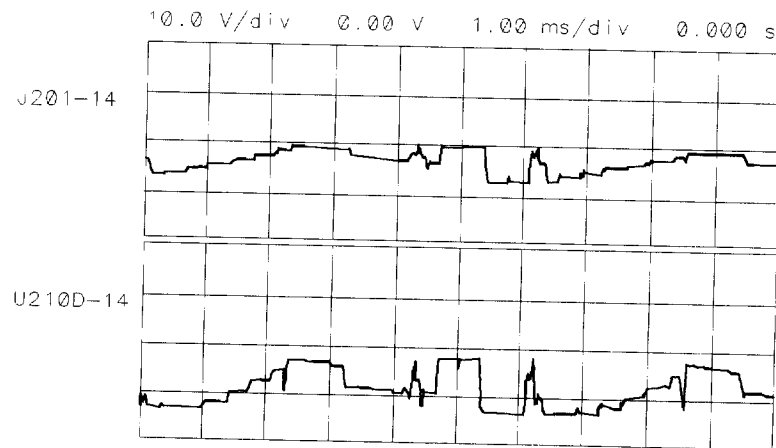
|                 |       |          |
|-----------------|-------|----------|
| Amplitude scale | ..... | 10 V/div |
| Sweep time      | ..... | 1 ms/div |
| Triggering      | ..... | External |
4. Externally trigger the oscilloscope off the signal at A2U207 pin 8 (LBRIGHT).
5. The waveforms should look like those illustrated in Figure 9-9. If the waveform at J201 pin 2 is bad, troubleshoot the X line generator (function block D of the A2 controller schematic, sheet 1 of 4).
6. If the waveform at U210D pin 14 is bad, troubleshoot the Z output circuit (function block M of A2 controller schematic, sheet 1 of 4).
7. Remove the short from J201 pin 13 to ground. Short A2J201 pin 1 to ground.



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**Figure 9-9. Delta X Waveform**

8. Move the oscilloscope's channel A probe to J201 pin 14.
9. The waveforms should look like those illustrated in Figure 9-10. If the waveform at J201 pin 14 is bad, troubleshoot the Y line generator (function block I of A2 controller schematic, sheet 1 of 4).
10. If the waveform at U210D pin 14 is bad, troubleshoot the Z output circuit (function block M of A2 controller schematic, sheet 1 of 4).
11. Remove the jumpers.

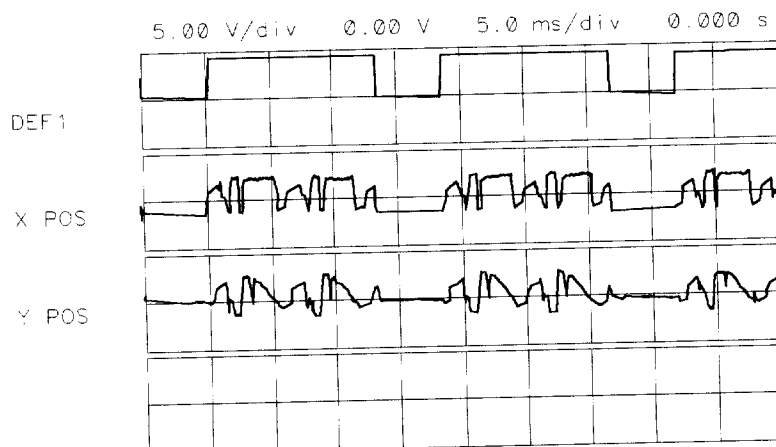


SK199

**Figure 9-10. Delta Y Waveform**

## Analog Zero-Span Problems

1. On the HP 8560E press **PRESET**, **SPAN**, **ZERO SPAN**, **SWEEP**, 1, **ms**, **CAL**, **MORE**, and **CRT ADJ PATTERN**.
2. Set an oscilloscope to the following settings:  
 Amplitude scale ..... 10 V/div  
 Sweep time ..... 1 ms/div  
 Triggering ..... External
3. Externally trigger the oscilloscope off the signal at A2U207 pin 8 (LBRIGHT).
4. The display should be similar to Figure 9-11 except that the untriggered trace should show at the left edge of the screen. In these settings, DEF1 causes switching between the line generators and the analog inputs (sweep and video). DEF1 remains high when the CRT adjust pattern is on. Refer to function block M of the A2 controller schematic, 1 of 4.
5. The sweep input from J1-41 should go from 0 V to +10 V; the video In signal should go from about 0 V to 1 V from the bottom to the top of the screen. Apply a dc voltage to A2J4, Video In, to test the circuit.
6. In Figure 9-11, there is no synchronization between DEF1 and the video patterns X POS and Y POS when DEF1 is TTL high. The Y POS level when DEF1 is low is the Video In level.



SK1100

**Figure 9-11. DEF1 Synchronization**

## Frequency-Count Marker Problems

The FREQ COUNT function works by dividing the 10.7 MHz IF signal by two (prescaling) and counting the divided-down signal using the frequency counter on the A2 controller assembly (block Z of the A2 schematic diagram). The prescaler is on the A4 Log amplifier/cal oscillator assembly (block Q of the A4 schematic diagram). Perform the following steps to determine whether the problem is on the A4 log amplifier/cal oscillator or A2 controller assembly:

1. Disconnect W53 from A2J7.
2. Connect the output of a synthesized source, such as an HP 3335A, to A2J7.
3. Set the synthesized source to the following settings:  
Amplitude ..... +10 dBm  
Frequency ..... 5.35 MHz
4. Set the HP 8560E to the following settings:  
Center frequency ..... 300 MHz  
Span ..... 1 MHz
5. On the HP 8560E press **FREQ COUNT**. The frequency counter actually reads one half the frequency of the 10.7 MHz IF. If the CNT frequency display reads all asterisks, the frequency counter is probably at fault.
6. If a valid frequency is displayed, troubleshoot the prescaler on the A4 log amplifier/cal oscillator assembly.
7. Reconnect W53 to A2J7.

## Frequency Counter

See function block Z of A2 schematic diagram (sheet 4 of 4) in the *HP 8560 E-Series Spectrum Analyzer Component Level Information*.

The frequency counter counts the frequency of the last IF and provides accurate timing signals for digital zero-spans. The circuit also provides timing signals to the A3 interface assembly's ADC (analog to digital converter). The nominal input frequency is 5.35 MHz (10.7 MHz divided by 2). The circuit's frequency reference in the frequency count mode is the 10 MHz reference from the A15 RF assembly. The frequency reference in digitized zero spans (sweep times  $\geq 30$  ms) is the 4 MHz HPIB\_CLK, selected by MUX U704.

In the frequency count mode, U702 prescales the 10 MHz reference by 5 to generate a 2 MHz timebase. This timebase feeds through MUX U704 to programmable-timer U700's CLK2 input. Programmable-timer U700's output (OUT2) is the gating signal (HBKT\_PULSE) for performing the frequency count. The gating time interval is a function of the counter resolution which may be set between 10 Hz and 1 MHz. Table 9-2 lists the gate time for each setting of COUNTER RES. The gate time is the period during which U511 pin 3 is high.

The FREQ COUNT input, A2J7, is gated in U511B by HBKT\_PULSE. The gated signal clocks divide-by-16 counters U703A and U703B. These counters are cascaded to form a divide-by-256 counter. The MSB of this counter, CD7, clocks the CLK0 input of U700. The frequency of CD7 is a function of COUNTER RES as shown in Table 9-2. If timer U700 overflows, OUT0 will be set and U701B clocked, generating CNTOVFLIRQ, which will interrupt the CPU.

If IRQAK2 is high, HBKT\_PULSE will clock U701A, generating FREQCNTLIRQ. Upon receiving the FREQCNTLIRQ interrupt, the CPU latches the CD0 to CD7 onto the BID bus by setting LCDRD (low counter data read) low and reading the counter data from the BID bus. The CPU will also read the data from the timer, U700, by setting L8254CS and LCNTLRD low, placing the timer data on the BID bus. The CPU resets U701A by setting IRQAK2 low via the BID bus and latch U506.

**Table 9-2. Gate Times**

| Counter Res                                        | Gate Time*<br>(U511 pin 3 high state) | A2TP16 | A2TP15   |
|----------------------------------------------------|---------------------------------------|--------|----------|
| 10 Hz                                              | 200 ms                                | 2 MHz  | 4.18 kHz |
| 100 Hz                                             | 20 ms                                 | 2 MHz  | 418 Hz   |
| 1 kHz                                              | 2 ms                                  | 2 MHz  | 41.8 Hz  |
| 10 kHz                                             | 2 ms                                  | 2 MHz  | 41.8 Hz  |
| 100 kHz                                            | 2 ms                                  | 2 MHz  | 41.8 Hz  |
| 1 MHz                                              | 2 ms                                  | 2 MHz  | 41.8 Hz  |
| * TP15 = (FREQ COUNT input $\times$ Gate Time)/256 |                                       |        |          |

1. Disconnect W22 from A2J8.
2. If a 10 MHz, TTL-level signal is not present at the end of W22 continue with step 3. If a 10 MHz signal is present at W22, proceed as follows:
  - a. Reconnect W22 to A2J8.
  - b. Set the HP 8560E to the following settings:
 

|                  |           |
|------------------|-----------|
| Span .....       | Zero span |
| Sweep time ..... | 20 ms     |
  - c. Monitor the signal at A2J2 pin 21. This is an output of the frequency counter, HBUCKET PULSE.
  - d. If HBUCKET PULSE is stuck high, troubleshoot the frequency counter.
3. Check for a 10 MHz signal at A15J302. If the signal is not present at A15J302, the A15 RF assembly is probably defective.

---

## State- and Trace-Storage Problems

State storage is in the two of the four Program RAMs and trace storage is in the two display RAMs. With low battery voltage, it is normal for states and traces to be retained if the power is off for less than one minute. If the power is left off for more than thirty minutes with low battery voltage, the stored states and traces will be lost. The following steps test battery backup:

1. Measure the voltage on W6 at A2J10. If the voltage is less than 2.6 V, check the BT1 battery.
2. If the battery voltage is correct, reconnect W6 to A2J10, set the spectrum analyzer's power off and wait five minutes.
3. Measure the voltage at A2U101 pin 28 and A2U102 pin 28.
4. If the voltage is less than 2.0 Vdc, the RAM power battery-backup circuitry on the A2 controller assembly is probably at fault.

## Keyboard Problems

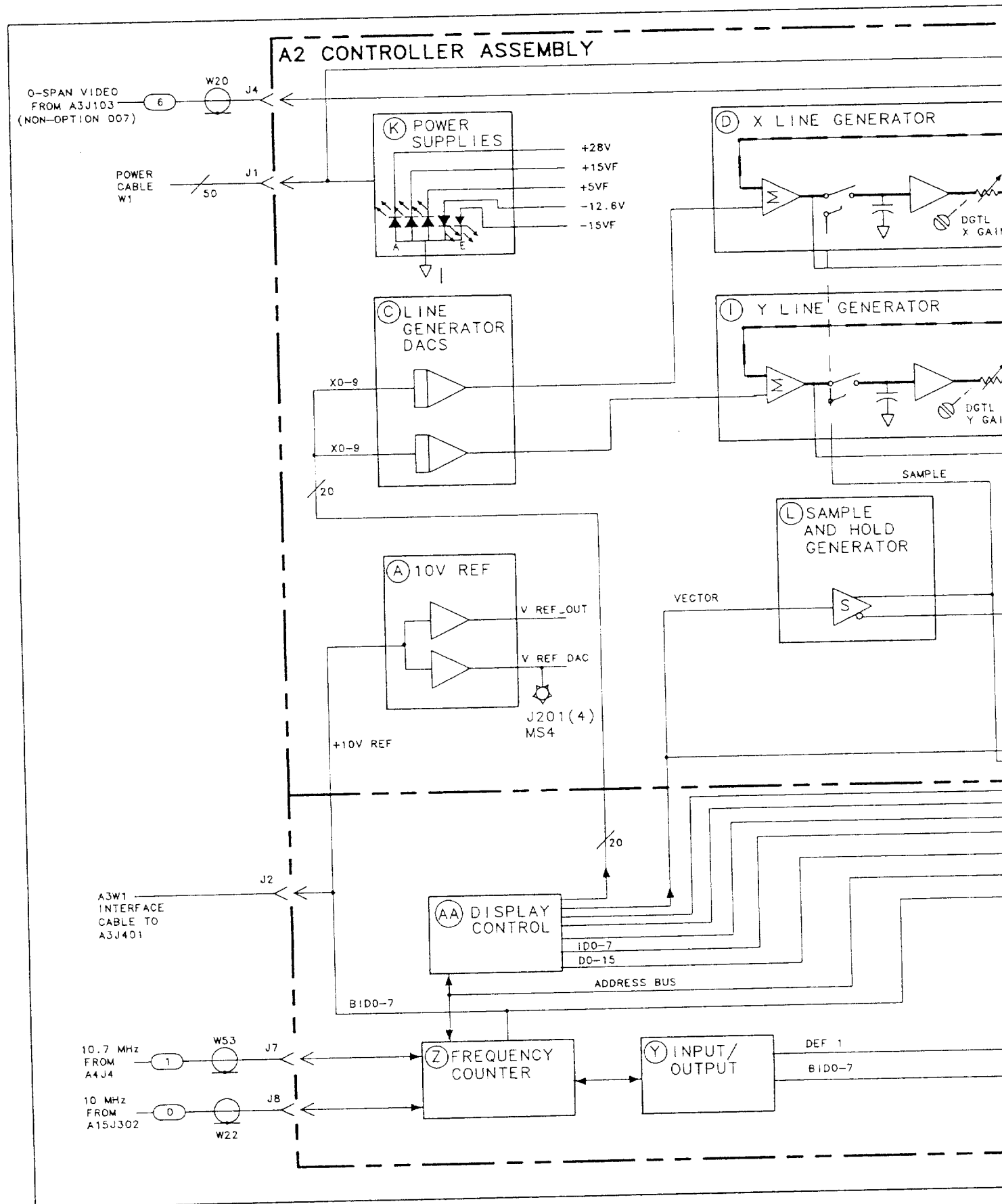
If the spectrum analyzer does not respond to keys being pressed or the knob being rotated, the fault could be either on the A3 interface assembly or the A2 controller assembly. To isolate the A2 controller assembly, use the following procedure. This procedure tests the spectrum analyzer response over HP-IB and the keyboard/RPG interrupt request signal.

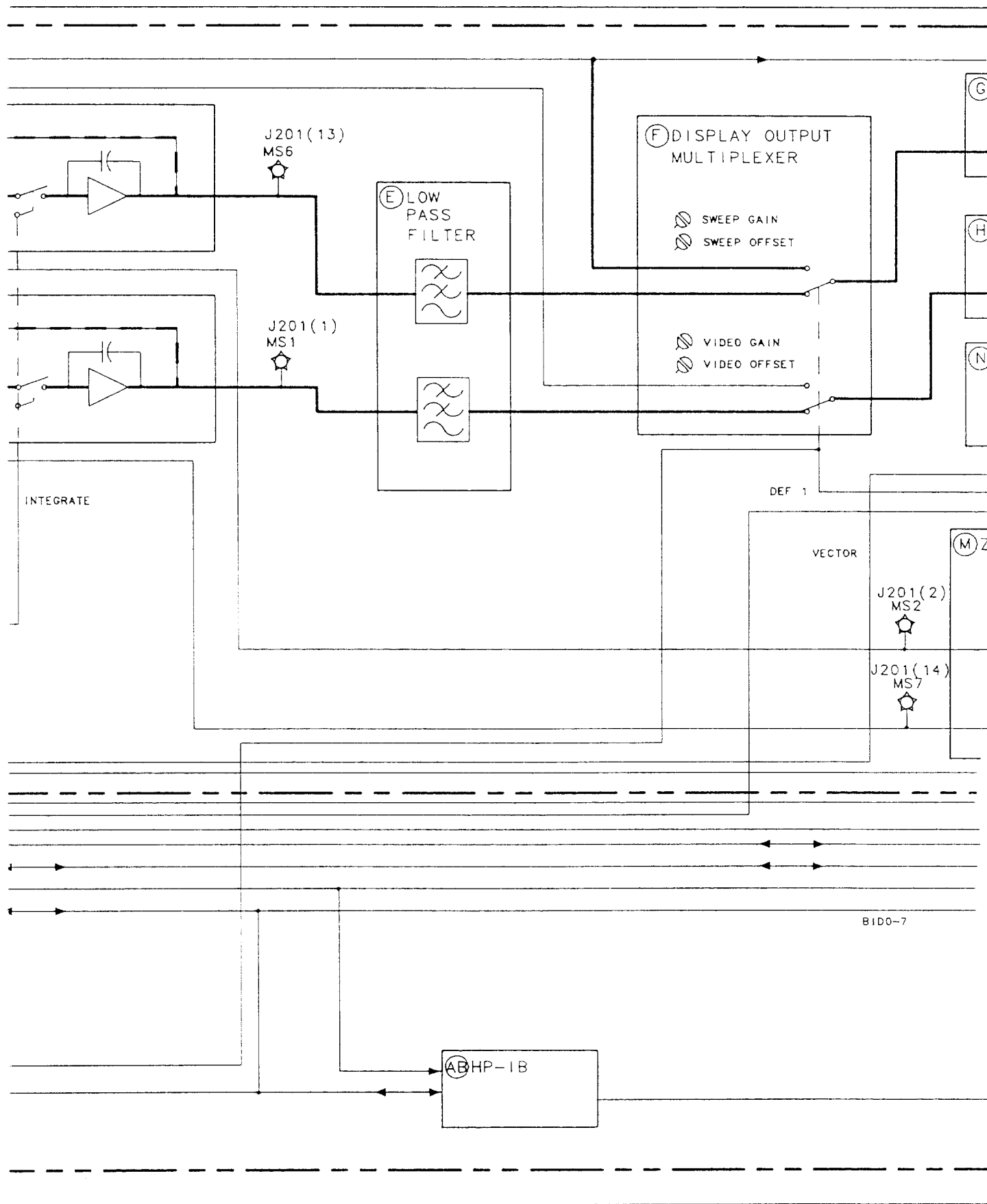
1. Enter and run the following BASIC program.

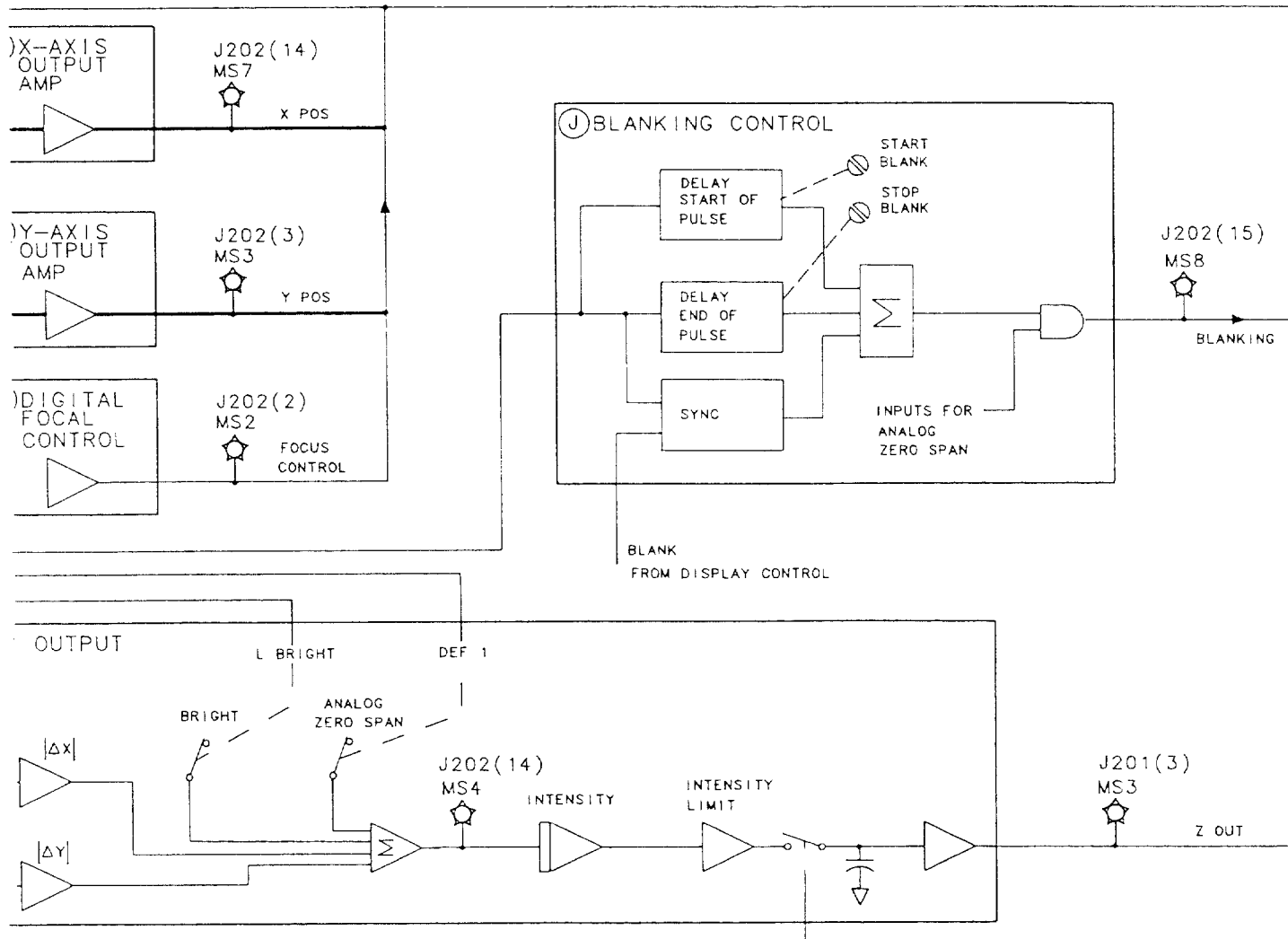
```
10 OUTPUT 718; "IP; SP 1 MHz;"
20 WAIT 2 ! Wait 2 seconds
30 OUTPUT 718; "AT 70 DB;"
40 WAIT 2 ! Wait 2 seconds
50 OUTPUT 718; "AT 30 DB;"
60 WAIT 2 ! Wait 2 seconds
70 OUTPUT 718; "AT 10 DB;"
80 END
```

2. When the program runs, three or four clicks should be heard. This is the A9 input attenuator changing attenuation value.
3. If the display shows the spectrum analyzer to be in RMT and the ATTEN value displayed on the CRT changed according to the program, the A2 controller assembly is working properly. Refer to Chapter 7, "ADC/interface."
4. If there was no response over HP-IB, the A2 controller is probably defective. Be sure to also check the A19 HP-IB assembly and A19W1.
5. If there was an improper response (for example, the displayed ATTEN value changed but no clicks were heard), the A2 controller is probably working properly.
6. Attach a logic probe to A2U2 pin 2. Look for pulses while pressing a key and rotating the knob (RPG). This is the interrupt request signal for the keyboard and RPG.
7. If the interrupt request signal is always low, troubleshoot the A2 controller assembly.
8. If the interrupt request signal is always high, the fault is on either the A3 interface or A1A1 keyboard assembly.

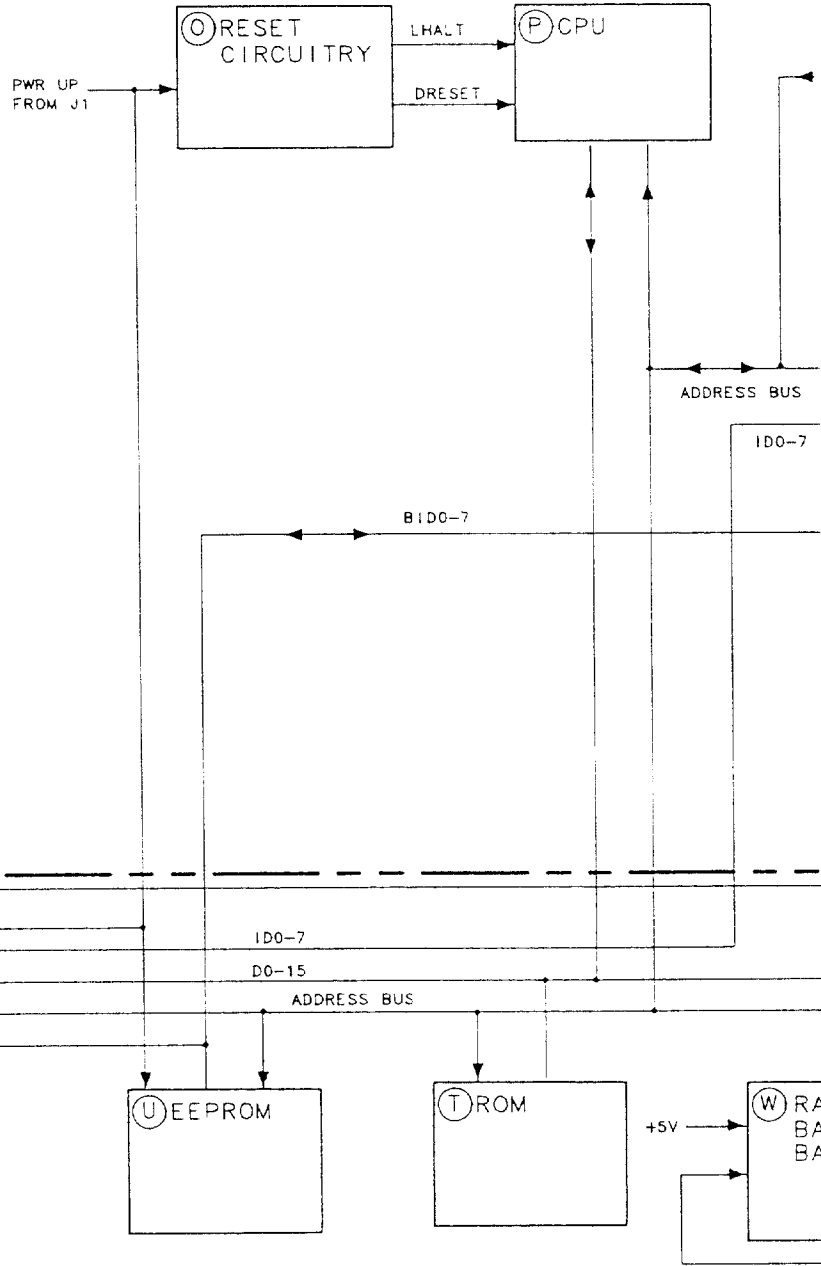








SHEET 1 OF 4



SHEET 4 OF 4

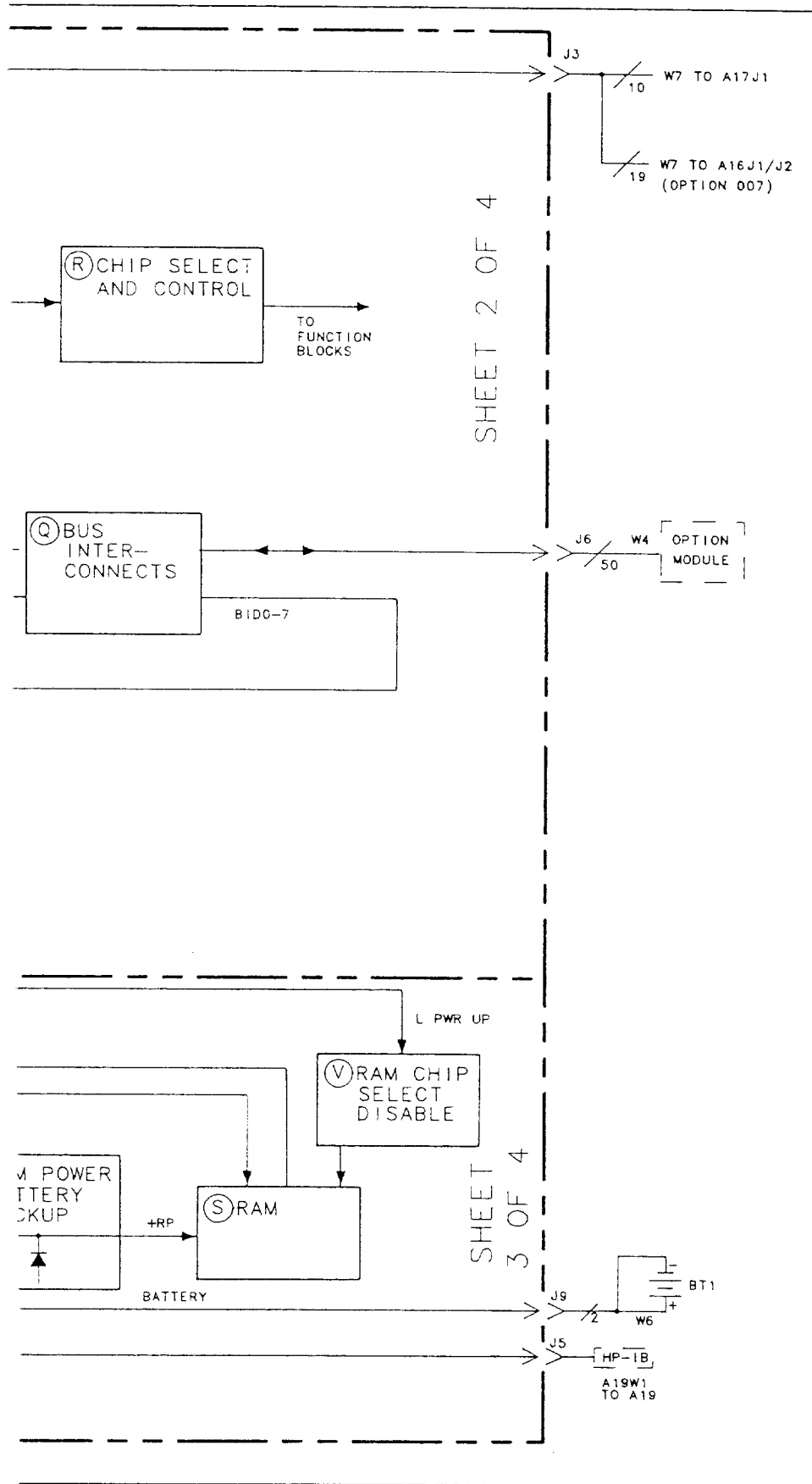


FIGURE 9-12. A2 CONTROLLER BLOCK DIAGRAM

## Synthesizer Section

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The synthesizer section includes the A7 first LO distribution amplifier, A11 YTO, and parts of the A14 frequency control and A15 RF assemblies. Simplified and detailed block diagrams for each assembly are located at the end of this chapter.

- Synthesizer Troubleshooting Section
  - Test Setup Troubleshooting
  - Troubleshooting Using the TAM
  - General PLL Troubleshooting
    - PLL Locked at Wrong Frequency
    - Unlocked PLL
  - Unlocked Reference PLL (100 MHz VCXO)
    - Operation (100 MHz VCXO)
    - Troubleshooting (100 MHz VCXO)
    - Third LO Driver Amplifier (100 MHz VCXO)
  - Unlocked Reference PLL (600 MHz SAWR)
    - Operation (600 MHz SAWR)
    - Troubleshooting (600 MHz SAWR)
    - Third LO Driver Amplifier (600 MHz SAWR)
  - Unlocked Offset Lock Loop (Sampling Oscillator)
    - Operation
    - Troubleshooting
  - Unlocked YTO PLL
    - Operation
    - Troubleshooting an Unlocked YTO PLL
  - Unlocked Fractional N PLL
    - Operation
    - Confirming an Unlocked Condition
  - Fractional N PLL
  - Frequency Span Accuracy Problems
    - Determining the First LO Span
    - Confirming Span Problems
  - YTO Main Coil Span Problems (LO Spans >20 MHz)
    - YTO FM Coil Span Problems (LO Spans 2.01 MHz to 20 MHz)
    - Fractional N Span Problems (LO Spans  $\leq 2$  MHz)
    - First LO Span Problems (All Spans)
  - Phase Noise Problems
    - Phase Noise in Locked versus Unlocked Spans
    - Reference versus Reference PLL Phase Noise
    - Fractional N versus Offset PLL or YTO PLL Phase Noise
    - Fractional N PLL Phase Noise
  - Sampler and Sampler IF
  - Sweep Generator Circuit
  - A21 OCXO

---

|                |                                                                                                                                                                                                        |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Caution</b> | All of the assemblies are extremely sensitive to electrostatic discharge (ESD). For further information regarding electrostatic cautions, refer to “Electrostatic Discharge Information” in Chapter 1. |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

---

|                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Caution</b> | Using an active probe, such as an HP 85024A, with a spectrum analyzer is recommended for troubleshooting the RF circuitry. If an HP 1120A active probe is being used with a spectrum analyzer, such as the HP 8566A/B, or HP 8569A/B having dc coupled inputs, either set the active probe for an ac coupled output or use a dc blocking capacitor (HP 11240B) between the active probe and the spectrum-analyzer input. Some spectrum analyzers can be set to ac coupled. Failure to do this can result in damage to the spectrum analyzer or the probe. |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

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## Synthesizer Troubleshooting Section

The A11 YTO (the HP 8560E's first LO) is a YIG-tuned oscillator which tunes from 2.95 to 6.8107 GHz. The A7 LO distribution amplifier (LODA) levels A11's output and distributes the signal to the A8 low band mixer, A10 YIG-tuned mixer/filter, A15U100 sampler, and the front panel's 1ST LO OUTPUT. The synthesizer section includes the following PLLs (Phase Locked Loops):

|                                      |                                 |
|--------------------------------------|---------------------------------|
| YTO PLL                              | A7, A11, A14 and A15 assemblies |
| Offset PLL (sampling oscillator PLL) | A15 RF assembly                 |
| Fractional N PLL                     | A14 frequency control assembly  |
| Reference PLL                        | A15 RF assembly                 |

The fractional N PLL is sometimes swept backwards (higher frequency to lower frequency). This is necessary because of the way in which the sampler IF signal is produced.

- 
- |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note</b> | <ul style="list-style-type: none"><li>■ The frequency control board is digitally controlled. If multiple failures appear in unrelated areas of the circuitry, the control may be at fault. Refer to the troubleshooting procedures in this chapter for further help on isolating those failures.</li><li>■ The TAM tests the signal path circuitry by digitally controlling the hardware and monitoring the control lines to make sure they are responding properly. Use the TAM's automatic fault isolation routine or verify the RF levels manually to ensure proper operation.</li></ul> |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
- 

### Check A3 ADC MUX function block (steps 1-4)

1. Connect a DVM's positive lead to A15J200 pin 13 and the negative lead to A15J200 pin 6. This measures the sampling oscillator tune voltage which is an input to the A3 interface assembly's ADC MUX.

2. Set the HP 8560E to the following settings:

Span ..... 0 Hz  
Center frequency ..... 389.5 MHz  
Trigger ..... Single

3. Use the data entry keys to tune the **CENTER FREQ** to the values listed in Table 10-1.
4. As the sampling oscillator frequency is increased, the DVM reading should also increase. If the tune voltage is correct, but the ADC measures the voltage and determines it to be out of specification, troubleshoot the A3 assembly's ADC MUX.

**Table 10-1. Center Frequency Tuning Values**

| HP 8560E<br>Center Frequency (MHz) | Sampling<br>Oscillator's Frequency (MHz) |
|------------------------------------|------------------------------------------|
| 2156.3                             | 285.000                                  |
| 2176.3                             | 286.364                                  |
| 2199.5                             | 287.500                                  |
| 2230.3                             | 288.462                                  |
| 799.3                              | 288.889                                  |
| 2263.3                             | 290.000                                  |
| 2282.3                             | 290.909                                  |
| 2302.3                             | 291.667                                  |
| 2155.3                             | 292.500                                  |
| 2158.3                             | 293.478                                  |
| 2336.3                             | 294.444                                  |
| 2196.3                             | 295.000                                  |
| 1.3                                | 296.000                                  |
| 2378.3                             | 296.471                                  |
| 2410.3                             | 297.000                                  |
| 2422.3                             | 297.222                                  |

**Check A14J301 10 MHz reference input (steps 5-8)**

5. Disconnect W37 from A14J301.
6. Connect a test cable from W37 to the input of another spectrum analyzer. Tune the other spectrum analyzer to the following settings:  
Center frequency ..... 10 MHz  
Span ..... 2 MHz
7. The amplitude of the 10 MHz reference signal should measure  $>-1$  dBm. If the signal does not measure  $>-1$  dBm, troubleshoot A15's 10 MHz distribution and A21 OCXO (if not Option 103).
8. Reconnect W37 to A14J301.

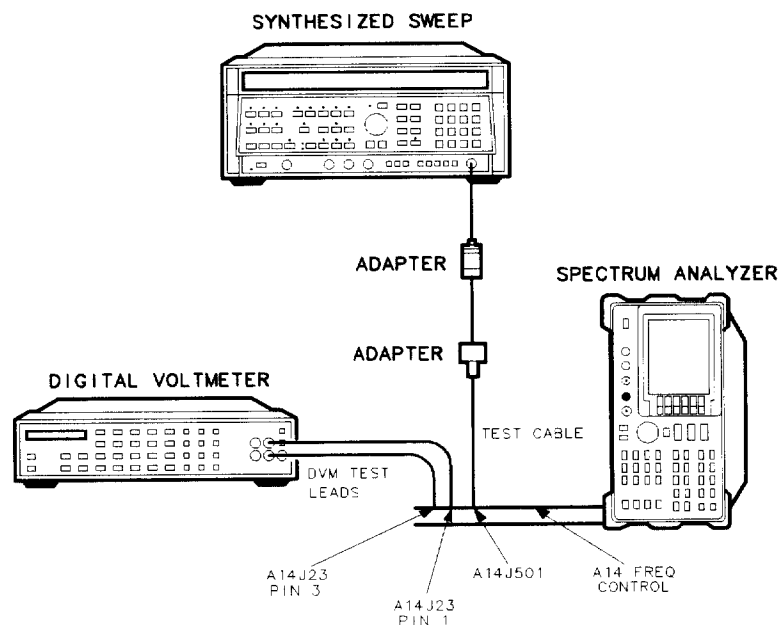
### Check first LO (steps 9-11)

9. Connect the CAL OUTPUT to INPUT 50Ω.
10. Set the HP 8560E to the following settings:  
Center frequency ..... 300 MHz  
Span ..... 100 MHz  
Trigger ..... CONT
11. If the first LO is present, a signal should be displayed at about -10 dBm (approximately ±20 MHz from the center frequency). If no signal is displayed and ERR 334 LO AMPL is not present, suspect the A7 LODA. If no signal is displayed and ERR 334 LO AMPL is present, check the A11 YTO as follows:
  - a. Set jumper A14J23 to the TEST position.
  - b. Set the HP 8560E to the following settings:  
Center frequency ..... 50 Hz  
CF step ..... 300 MHz  
Span ..... 0 Hz
  - c. Connect a power meter directly to the output of the A11 YTO.
  - d. Press the HP 8560E's step-up key and measure the YTO output power at each step.
  - e. Check that A11 YTO's output power is between +9 and +13 dBm.
  - f. Set jumper A14J23 to the NORM position and reconnect the A11 YTO.

### Check A14 frequency control assembly (steps 12-17)

12. On the HP 8560E press **PRESET**, **SPAN**, **ZERO SPAN**, **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, and **FRAC N FREQ**. Note the fractional N oscillator frequency. (Ignore the minus sign, if present.)  

Fractional N Oscillator Frequency = \_\_\_\_\_ MHz
13. Check A14J304 (FRAC N TEST) port with a spectrum analyzer for this exact frequency. The amplitude should be approximately -10 dBm.
14. Disconnect W32 from A14J501 and connect the output of a signal source to A14J501. Remove the jumper from A14J23. Connect a DVM's positive lead to A14J23 pin 1 and negative lead to A14J23 pin 3. See Figure 10-1.
15. Set the signal source to the following settings:  
Power ..... 0 dBm  
Frequency ..... Frequency recorded in step 12
16. Tune the source 1 kHz below the fractional N frequency. The voltage measured on the DVM should be approximately 12 Vdc.
17. Tune the source 1 kHz above the fractional N frequency. The voltage measured on the DVM should be approximately -12 Vdc.
18. If the DVM reading does not change, the A14 frequency control assembly is defective. Reconnect W32 to A14J501.



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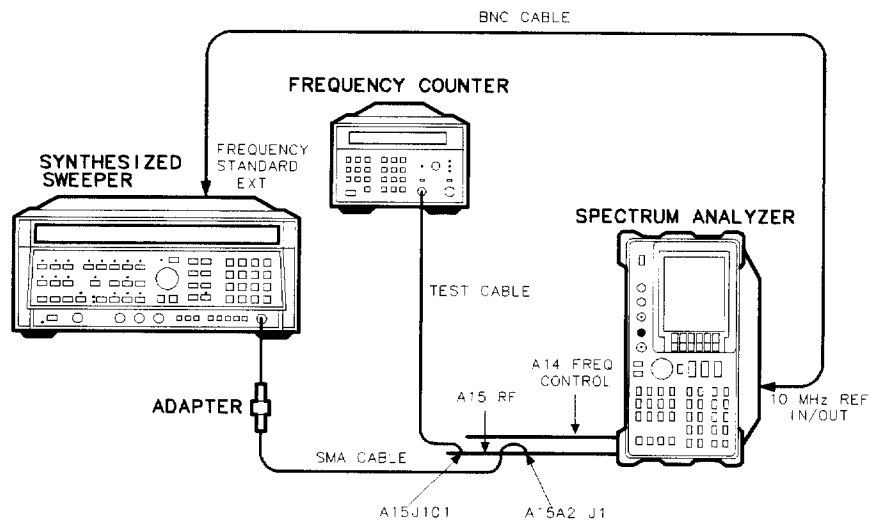
**Figure 10-1. YTO Loop Test Setup**

**Check A15 RF assembly (steps 18-25)**

19. Disconnect W34 from A15U100J1 and disconnect W32 from A15J101.
20. Connect a frequency counter to A15J101. Connect a high-frequency test cable from an HP 8340A/B synthesized sweeper to A15U100J1. See Figure 10-2.
21. Connect a BNC cable from the HP 8560E's 10 MHz REF IN/OUT to the HP 8340A/B's FREQUENCY STANDARD EXT input.
22. Set the HP 8340A/B to the following settings:
 

|                          |        |
|--------------------------|--------|
| Frequency standard ..... | EXT    |
| Power level .....        | -5 dBm |
23. Set the HP 8560E to the following settings:
 

|               |        |
|---------------|--------|
| Span .....    | 0 Hz   |
| Trigger ..... | Single |
24. Set the HP 8560E and HP 8340A/B frequencies to the combinations listed in Table 10-2 and press **SGL SWP** on the spectrum analyzer.



SK 1102

**Figure 10-2. Sampler and Sampling Oscillator Test Setup**

25. At each combination, the frequency counter should measure a sampler IF as shown in Table 10-2. (The offset PLL's sampling oscillator tunes to the frequencies listed in the table.) If the frequency counter does not read the indicated sampler IF  $\pm 10$  kHz, suspect the A15 RF assembly.
26. Reconnect W34 to A15U100J1 and W32 to A15J101.
27. The 1ST LO OUTPUT, located on the front panel, must be terminated in 50  $\Omega$ . If the YTO unlocks only with certain center frequency and span combinations, check that the termination is in place.
28. Set the HP 8560E's **CENTER FREQ** and **SPAN** to generate the unlock conditions.
29. On the HP 8560E press **SGL SWP**.
30. Move jumper A14J23 to the TEST position.
31. Disconnect W34 from A15U100J1 and measure the power of the signal at the end of W34.
32. If the power is less than  $-6.5$  dBm, suspect W34, A7 LODA, or A11 YTO.
33. Move jumper A14J23 to the NORM position.

**Table 10-2. Sampling Oscillator Test Frequencies**

| HP 8340A<br>CW Frequency<br>(GHz) | HP 8560E<br>Center Frequency<br>(MHz) | Offset PLL<br>Sampling Oscillator Freq<br>(MHz) | Counter Reading<br>Sampler IF<br>(MHz) |
|-----------------------------------|---------------------------------------|-------------------------------------------------|----------------------------------------|
| 6.067000                          | 2156.3                                | 285.000                                         | 82.000                                 |
| 6.087000                          | 2176.3                                | 286.364                                         | 73.364                                 |
| 6.110200                          | 2199.5                                | 287.500                                         | 72.700                                 |
| 6.141000                          | 2230.3                                | 288.462                                         | 83.308                                 |
| 4.710000                          | 799.3                                 | 288.889                                         | 87.778                                 |
| 6.174000                          | 2263.3                                | 290.000                                         | 84.000                                 |
| 6.193000                          | 2282.3                                | 290.909                                         | 83.909                                 |
| 6.213000                          | 2302.3                                | 291.667                                         | 88.000                                 |
| 6.066000                          | 2155.3                                | 292.500                                         | 76.500                                 |
| 6.069000                          | 2158.3                                | 293.478                                         | 94.044                                 |
| 6.247000                          | 2336.3                                | 294.444                                         | 63.667                                 |
| 6.107000                          | 2196.3                                | 295.000                                         | 88.000                                 |
| 3.912000                          | 1.3                                   | 296.000                                         | 64.000                                 |
| 6.289000                          | 2378.3                                | 296.471                                         | 63.118                                 |
| 6.321000                          | 2410.3                                | 297.000                                         | 84.000                                 |
| 6.333000                          | 2422.3                                | 297.222                                         | 91.333                                 |

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## Test Setup Troubleshooting

Some synthesizer section problems require placing the YTO PLL in an unlocked condition. This is done by moving jumper A14J23 to the TEST position. This grounds the YTO ERROR signal, disabling the CPU's ability to detect an unlocked YTO. The FM coil driver output is set to its mid-range level causing the YTO to be controlled only by the main coil tune DAC.

Synthesizer section troubleshooting is best done with the HP 8560E's SPAN set to 0 Hz (even though it is still possible to sweep the Main and FM coils of the YTO).

With the YTO in its unlocked conditions and the SPAN set to 0 Hz, the nominal YTO frequency is not necessarily the value listed as LO FREQ in the Frequency Diagnose menu. The YTO has an initial pretune accuracy of  $\pm 20$  MHz. To display the nominal YTO's frequency, press **[CAL]**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, **LO FREQ**.

The fractional N oscillator frequency is the same as the desired sampler IF. To display the fractional N oscillator frequency press **[CAL]**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, **FRAC N FREQ**. If the sampler IF is negative (YTO frequency is lower than the desired sampling oscillator harmonic), the fractional N frequency will be displayed as a negative number.

# Troubleshooting Using the TAM

When using automatic fault isolation, the TAM indicates suspected circuits that need to be manually checked. Use Table 10-4 to locate the manual procedure.

Table 10-5 lists assembly test connectors associated with each manual probe troubleshooting test. Figure 10-3 illustrates the location of A14 and A15 test connectors.

The pin locations of a 16-pin TAM connector are indicated in Figure 10-4. Table 10-3 indicates the correspondence between a measured signal line and the TAM connector pin.

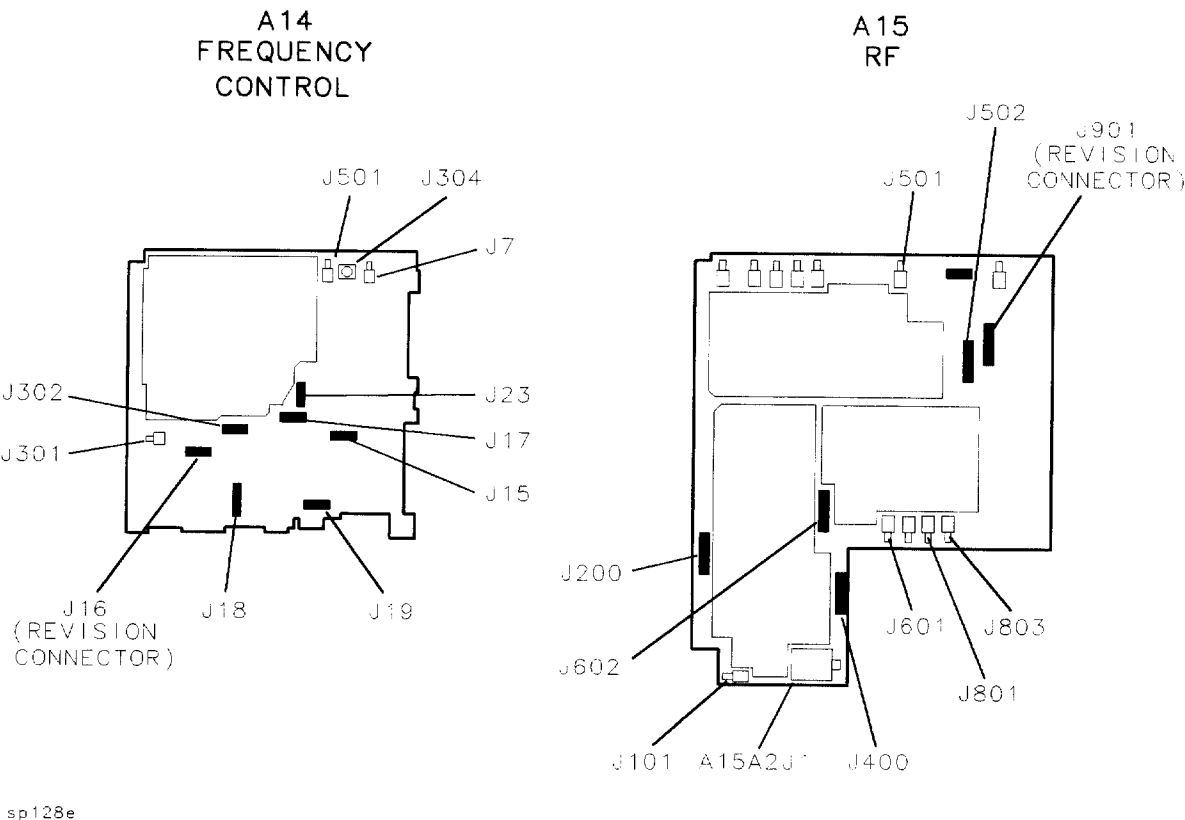
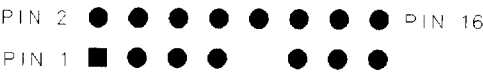


Figure 10-3. A14 and A15 Test Connectors



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Figure 10-4. TAM Connector Pin Locations

**Table 10-3. Measured Signal Line Location**

| Measured Signal Line | Connector Pin |
|----------------------|---------------|
| MSL1                 | pin 1         |
| MSL2                 | pin 2         |
| MSL3                 | pin 3         |
| MSL4                 | pin 4         |
| MSL5                 | pin 5         |
| GND                  | pin 6         |
| MSL6                 | pin 13        |
| MSL7                 | pin 14        |
| MSL8                 | pin 15        |

**Table 10-4. Automatic Fault Isolation References**

| Suspected Circuit Indicated<br>by Automatic Fault Isolation           | Manual Procedure to Perform                              |
|-----------------------------------------------------------------------|----------------------------------------------------------|
| Check the YTO loop                                                    | Confirming a Faulty Synthesizer Section<br>(steps 9-11)  |
| Check first LO                                                        | Unlocked YTO PLL (steps 10-13)                           |
| Check first LO pretune frequency and amplitude                        | Third LO Driver Amplifier (steps 1-6)                    |
| Check 3rd LO drive                                                    | Unlocked Reference PLL (steps 8-13)                      |
| Check 10 MHz reference to phase/frequency<br>detector                 | Unlocked Reference PLL (steps 12 and 13)                 |
| Check for 10 MHz signal at other input to<br>phase/frequency detector | Confirming a Faulty Synthesizer Section (steps<br>1-4)   |
| Check A3 ADC MUX function block                                       | Confirming a Faulty Synthesizer Section<br>(steps 12-17) |
| Check A14 frequency control assembly                                  | Confirming a Faulty Synthesizer Section<br>(steps 5-8)   |
| Check A14J301 10 MHz REF input                                        | Confirming a Faulty Synthesizer Section<br>(steps 18-25) |
| Check A15 RF assembly                                                 | First LO Span Problems (All Spans) (steps 14-21)         |
| Check current source                                                  | Unlocked YTO PLL (steps 28-34)                           |
| Check FM loop sense                                                   | Third LO Driver Amplifier (steps 1-6)                    |
| Check level at amplifier Input                                        | Unlocked Offset PLL (steps 3-13)                         |
| Check levels into mixer U400                                          | Unlocked Offset PLL (steps 1 and 2)                      |
| Check loop references                                                 | Unlocked YTO PLL (steps 45-49)                           |
| Check main coil tune DAC                                              | Unlocked YTO PLL (steps 41-44)                           |
| Check main coil coarse and fine DACs                                  | First LO Span Problems $\leq 2$ MHz (step 8)             |
| Check offset span accuracy                                            | Unlocked Reference PLL (steps 17-22)                     |
| Check phase/frequency detector                                        | Unlocked Offset PLL (steps 3-7, 14-19)                   |
| Check path to phase/frequency detector                                | Unlocked YTO PLL (steps 14-18)                           |
| Check fractional N oscillator                                         | Unlocked YTO PLL (steps 19-22)                           |
| Check sampler drive output of A7 LODA                                 | Unlocked YTO PLL (steps 23-27)                           |
| Check sampler IF                                                      | Sampler and Sampler IF (steps 1-15)                      |
| Check sampler/sampler IF operation                                    | First LO Span Problems (All Spans) (steps 6-13)          |
| Check span attenuator                                                 | Sweep Generator Circuit                                  |
| Check sweep generator                                                 | Unlocked Reference PLL (steps 23-26)                     |
| Check the 600 MHz reference loop amplifier                            | Unlocked YTO PLL                                         |
| Check the YTO loop                                                    | First LO Span Problems (2.01 MHz to 20 MHz)<br>(step 6)  |
| Check YTO FM coil driver                                              | Unlocked YTO PLL (steps 35-40)                           |
| Check YTO FM coil driver and main loop<br>error voltage driver        |                                                          |

**Table 10-5. TAM Tests versus Test Connectors**

| Connector                                                                                      | Manual Probe Troubleshooting Test | Measured Signal Lines |
|------------------------------------------------------------------------------------------------|-----------------------------------|-----------------------|
| A14J15                                                                                         | Sweep generator                   | MS8                   |
|                                                                                                | Span attenuator DAC               | MS7                   |
|                                                                                                | Span attenuator switches          | MS7                   |
|                                                                                                | Sweep + tune mult input amp       | MS1, OS1              |
|                                                                                                | Sweep + tune mult input switches  | MS1, MS3              |
| A14J16                                                                                         | FAV generator                     | MS4                   |
|                                                                                                | FAV gen 0.5 V/GHz output          | MS5                   |
| A14J17                                                                                         | Main coil coarse DAC              | MS3                   |
|                                                                                                | Main coil fine DAC                | MS2                   |
|                                                                                                | Main coil DACs output             | MS5                   |
|                                                                                                | Main loop error volt DVR          | MS4                   |
|                                                                                                | Option drive                      | MS8                   |
|                                                                                                | Option drive switch               | MS7                   |
|                                                                                                | Option drive DAC                  | MS6                   |
| A14J18                                                                                         | $\pm 10$ V reference              | MS1, MS2              |
|                                                                                                | LODA drive                        | MS5, MS6, MS7, MS8    |
|                                                                                                | Main coil tune DAC                | MS3                   |
|                                                                                                | Sweep gen DAC                     | MS4*                  |
|                                                                                                | Sweep gen DAC                     | MS4*                  |
| A14J19                                                                                         | Second conv PIN switch            | MS8                   |
|                                                                                                | Second conv mixer bias            | MS1                   |
|                                                                                                | Second conv drain bias            | MS3                   |
|                                                                                                | Second conv doubler bias          | MS4                   |
|                                                                                                | Second conv driver bias           | MS5                   |
|                                                                                                | First mixer drive switch          | MS7                   |
|                                                                                                | First mixer drive DAC             | MS6                   |
| A14J302                                                                                        | Revision                          | MS7                   |
|                                                                                                | Fractional N out                  | MS1                   |
|                                                                                                | Divided reference                 | MS4                   |
|                                                                                                | Feedback buffer bias              | MS5                   |
|                                                                                                | Outamp bias                       | MS6                   |
| * Only on A14 assemblies with part numbers 08560-60059, 08560-69059, 08560-60062, 08560-69062. |                                   |                       |

**Table 10-5. TAM Tests versus Test Connectors (continued)**

| Connector | Manual Probe Troubleshooting Test  | Measured Signal Lines |
|-----------|------------------------------------|-----------------------|
| A15J200   | Positive 15 volt supply            | MS1                   |
|           | Sampler drive buffer bias          | MS2                   |
|           | Sampling oscillator bias           | MS3                   |
|           | Offset lock drive buffer           | MS4                   |
|           | OFL error voltage                  | MS6                   |
|           | Negative 10 volt supply            | MS8                   |
|           | Offset lock loop BW DAC            | MS5,MS7,MS8           |
| A15J400   | Positive 15 volt supply            | MS2                   |
|           | Offset lock RF buffer              | MS4                   |
|           | IF AMP/limiter bias                | MS6                   |
|           | Offset lock loop buffer D          | MS7                   |
|           | Offset lock loop buffer C          | MS8                   |
|           | Sampler bias test                  | MS3                   |
| A15J502   | Positive 15 volt supply            | MS2                   |
|           | Third LO tune voltage              | MS3                   |
|           | Offset lock loop buffer            | MS4                   |
|           | 600 MHz oscillator bias            | MS5                   |
|           | Calibrator AGC amp bias            | MS6                   |
|           | Calibrator ampl adj                | MS7                   |
|           | 3rd LO driver amp                  | MS1, MS8              |
| A15J602   | Positive 15 volt supply            | MS8                   |
|           | Flatness compensation 3            | MS2                   |
|           | Flatness compensation 2            | MS5                   |
|           | Flatness compensation 1            | MS6                   |
|           | SIG ID collector bias (Option 008) | MS7                   |
|           | RF gain control test               | MS1, MS3              |
| A15J901   | Revision                           | MS3                   |
|           | External mixer switch              | MS1, MS8              |
|           | Signal ID switch (Option 008)      | MS5, MS6              |
|           | Ten volt reference                 | MS4                   |
|           | External mixer bias                | MS7                   |

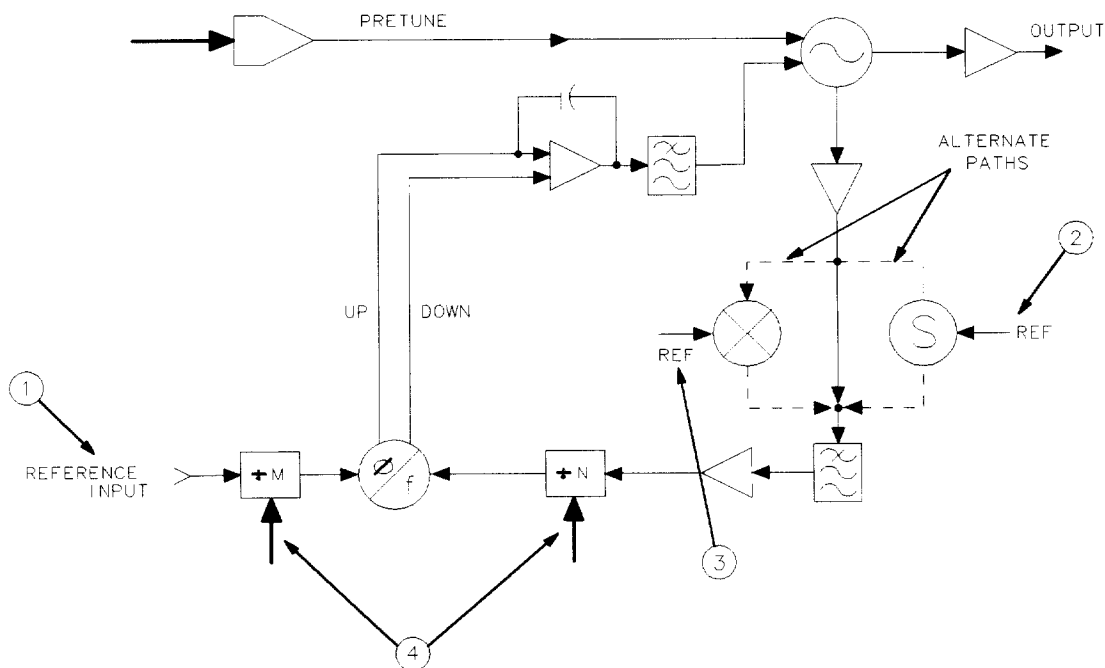
## General PLL Troubleshooting

The synthesizer section relies heavily on phase-locked loops (PLL). Typically, faulty PLL's are either locked at the wrong frequency or unlocked. The information below applies to troubleshooting these two classes of problems on a generalized PLL.

### PLL Locked at Wrong Frequency

Numbers in the following text identify items in Figure 10-5.

- Any frequency errors at reference (1) will be multiplied by  $N/M$  on the PLL's output.
- A sampler reference-frequency error (2) will be multiplied by its harmonic on the PLL's output.
- A mixer reference-frequency error (3) produces the identical error on the PLL's output.
- If divider input or output frequencies (4) are wrong, check for incorrect divide numbers and data controlling the dividers.



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**Figure 10-5. PLL Locked at Wrong Frequency**

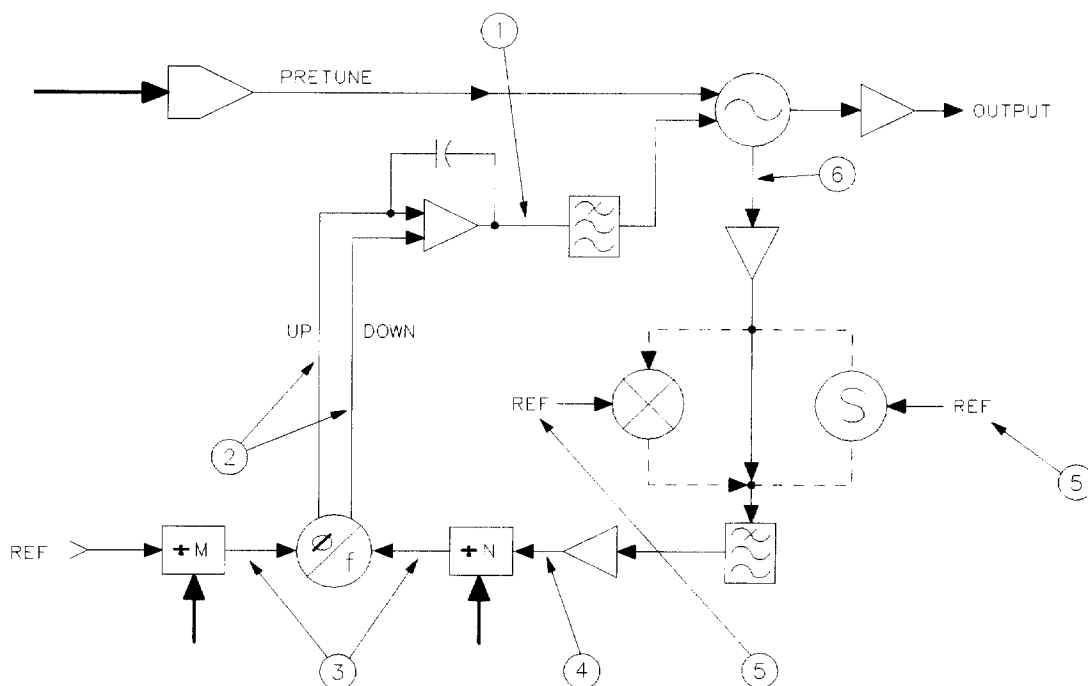
## Unlocked PLL

An unlocked PLL can be caused by problems inside or outside the PLL. Troubleshoot this problem by working backward from the oscillator as described in the steps below. Numbers in the following text identify items in Figure 10-6.

1. The loop integrator's output voltage (1) should be attempting to tune the oscillator to the correct frequency.

The voltage at (1) should increase as the frequency increases on all of the PLLs:

| PLL              | Measurement Point        |
|------------------|--------------------------|
| YTO PLL          | A14J23 pin 1 (YTO ERROR) |
| Reference PLL    | A15J502 pin 3 (LO3 ERR)  |
| Sampler PLL      | A15J200 pin 13 (OFL ERR) |
| Fractional N PLL | A14TP13 (INTEGRATOR)     |



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**Figure 10-6. Unlocked PLL**

2. If the integrator's output voltage changes in the manner described in step 1, the problem is external to the PLL. For example, the reference frequency could be faulty. If the integrator's output voltage appears incorrect, confirm that the pulses out of the phase detector (2) are attempting to tune the oscillator in the correct direction.

3. If the phase detector's output is bad, check the inputs to the detector (3). One input should be higher in frequency than the other; this should match the phase detector outputs.
4. Confirm proper power levels for the signals at the input to the "N" dividers (4), the reference inputs (5 and 7), and the loop's feedback path (6).

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## Unlocked Reference PLL (100 MHz VCXO)

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**Note** The following information is for A15 RF assemblies 08563-60054, 08563-60055, and 08563-60056. For earlier A15 RF assemblies, proceed to *Unlocked Reference PLL (600 MHz SAWR)* in this chapter.

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### Operation (100 MHz VCXO)

The 600 MHz reference is generated by tripling, then doubling the output of the 100 MHz phase-locked loop. If the 600 MHz reference is off frequency, the 100 MHz phase-lock circuitry is probably at fault. If there is no signal present at A15J701, or if the level is less than  $-3$  dBm, the 100 MHz VCXO, the tripler, or the doubler circuitry has probably failed. Refer to function blocks Q, R, and S of the A15 RF schematic (08563-90071, 08563-90072, or 08563-90073) sheet 2 of 4 in the *HP 8560 E-Series Spectrum Analyzer Component Level Information* binder.

### Troubleshooting (100 MHz VCXO)

#### Check 100 MHz VCXO, tripler, and doubler (steps 1-7)

1. Using an active probe/spectrum analyzer combination, such as the HP 85024A/HP 8566B, measure the tripler output at A15TP700. The tripler output should be  $+3$  dBm  $\pm 2$  dB.
2. If the tripler output is within tolerance, suspect the doubler circuitry. Refer to function block S of the A15 RF schematic.
3. If the tripler output is too low, probe the output of A15U700 RF amplifier. The level should be  $+16.5$  dBm  $\pm 2$  dB. The level at the input of A15U700 should be  $+8.5$  dBm  $\pm 2$  dB.
4. If the level at the input of A15U700 is too low, suspect a faulty 100 MHz VCXO. Refer to function block Q of the A15 RF schematic.
5. On the spectrum analyzer, press **AUX CTRL**, **REAR PANEL**, and **10 MHz INT**.
6. Measuring the tune voltage indicates if the 100 MHz PLL is locked. Connect the ground lead the voltmeter to A15J1 pin 3 and measure the voltage at A15J700 pin 3.
7. The tune voltage should be between  $+1$  and  $+24$  Volts. If the tune voltage is incorrect, place the P700 jumper (on A15J700) in the TEST position (pin 1 to pin 2). This sets the tune voltage for varactor A15CR700 to the nominal  $+13$  Volts, making it easier to troubleshoot the 100 MHz VCXO, tripler, and doubler. Remember to return P700 jumper to the NORMAL position when you have finished troubleshooting the oscillator circuitry.

8. If the 100 MHz oscillator is working, the reason for the unlocked condition is either a problem in the 10 MHz reference or a fault in the signal path around the loop.

**Check 10 MHz reference to phase/frequency detector (steps 9-14)**

9. On the spectrum analyzer, press **AUX CTRL**, **REAR PANEL**, and **10 MHz INT**.
10. Check the 10 MHz reference frequency-accuracy by connecting a frequency counter to A15J301 and verify that the reference frequency is 10 MHz  $\pm$ 40 Hz after a 5 minute warm-up period.
11. If a 10 MHz signal  $>1$  V peak-to-peak is not present at A15J301, refer to the "10 MHz Reference" in Chapter 11.
12. Measure the signal at TP301 with an oscilloscope. Refer to function block M of A15 RF schematic.
13. Measure the signal at U502 pin 11 with an oscilloscope. Refer to function block X of A15 RF schematic. This signal should be TTL levels at 10 MHz with a 60 percent duty cycle.
14. If TTL-level signals (approximately 10 MHz) are not present, check signals backwards through the loop to find a fault in the signal path.
15. Measure the signals at the following test points with an active probe/spectrum analyzer combination:

|                              |                              |
|------------------------------|------------------------------|
| Junction of<br>C570 and C571 | 100 MHz, +2.5 dBm $\pm$ 2 dB |
|------------------------------|------------------------------|

|                                           |                            |
|-------------------------------------------|----------------------------|
| Junction of R715,<br>R716, R567, and R568 | 100 MHz, -3 dBm $\pm$ 2 dB |
|-------------------------------------------|----------------------------|

|            |                               |
|------------|-------------------------------|
| U700 pin 3 | 100 MHz, +16.5 dBm $\pm$ 2 dB |
|------------|-------------------------------|

|            |                              |
|------------|------------------------------|
| U700 pin 1 | 100 MHz, +8.5 dBm $\pm$ 2 dB |
|------------|------------------------------|

16. If an approximately 10 MHz TTL signal is present at U502 pin 11 with 60 percent duty cycle, and the RF portion of the phase-lock loop is functioning, the fault probably lies in the phase/frequency detector or the 100 MHz lock loop integrator.

### Check phase/frequency detector (steps 17-22)

17. Monitor U504 pin 5 and U503 pin 9 with an oscilloscope. These are the two outputs of the phase/frequency detector. Refer to function block O of A15 RF schematic.
18. A locked loop will exhibit stable, narrow (approximately 20 ns wide), and positive-going TTL pulses occurring at a 10 MHz rate at U504 pin 5 and U503 pin 9.
19. If the loop is unlocked, but signals are present on both inputs of the phase/frequency detector, the output pulses will be superimposed on each other.
20. If the loop is unlocked, and there is no signal at one of the phase/frequency detector inputs, one phase detector output will be at TTL low and the other will be at TTL high. For example, if there is no input signal at U504 pin 3, U504 pin 5 will be TTL low and U503 pin 9 will be TTL high. If there is no input signal at U503 pin 11, U503 pin 9 will be TTL low and U504 pin 5 will be TTL high.
21. To remove the 10 MHz reference input to the phase/frequency detector, press **AUX CTRL**, **REAR PANEL**, and **10 MHz EXT** with no signal applied to the rear-panel 10 MHz REF IN/OUT connector.
22. To remove the divided-down 100 MHz signal from the phase/frequency detector, short R595. Refer to function block X of A15 RF schematic.

### Check the 100 MHz lock loop integrator (steps 23-27)

23. Remove 10 MHz reference input to the phase/frequency detector by pressing **AUX CTRL**, **REAR PANEL**, and **10 MHz EXT**. No signal should be connected to the rear-panel 10 MHz REF IN/OUT connector.

---

|             |                                                                                                                                                                                                                          |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note</b> | The outputs of phase/frequency detector are low-pass filtered to reduce the 10 MHz component of the signal. The filtered signals are then integrated by U506 and the result is fed to the tune line of the 100 MHz VCXO. |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

---

24. Check that the voltage on A15J502 pin 3 is less than 0 Vdc. Refer to function block P of A15 RF schematic.
25. Press **AUX CTRL**, **REAR PANEL**, and **10 MHz INT** and remove the divided-down 100 MHz input to the phase/frequency detector by shorting R572.
26. Check that the voltage on A15J502 pin 3 is greater than 13 Vdc.
27. If the loop is locked, the voltage on A15J502 pin 3 should be between 0 and +6 Vdc.

28. If the front-panel CAL OUTPUT amplitude is out of specification and cannot be brought within specification by adjusting A15R561, CAL AMPTD, check the calibrator AGC amplifier with the following steps. Refer to function block W of A15 RF schematic.

---

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note</b> | The 300 MHz CAL OUTPUT signal comes from the tripled 100 MHz which is passed through a leveling loop. The 300 MHz signal passes through a low-pass filter for reducing higher harmonics. These harmonics can fool the detector. The 300 MHz signal passes through a variable attenuator controlled by PIN diode CR503 which is controlled by the feedback loop. Diode CR504 is the detector diode (the same type as CR505). Diode CR504 provides temperature compensation between the reference voltage and the detected RF voltage. |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

---

- a. Measure the level of 300 MHz at A15 TP505 with an active probe/spectrum analyzer combination. If the signal is less than +2 dBm, repeat the first 27 steps of this procedure.
  - b. If the signal at this point is correct, place a short across the PIN diode CR503.
  - c. If the signal level at the CAL OUTPUT is still less than -10 dBm with CR503 shorted out, troubleshoot the RF forward path through amplifier Q505. (The signal amplitude decreases.)
  - d. If the CAL OUTPUT signal level is greater than -10 dBm, troubleshoot the PIN diode attenuator, the detector, or the feedback path.
29. Measure the detector voltage at A15J502 pin 14. The voltage should measure approximately +0.3 Vdc when the CAL OUTPUT signal is at -10 dBm. This voltage should change with adjustment of A15R561, CAL AMPTD.
30. Check that the voltage at U507A Pin 3 is +1.7 Vdc. If this voltage is not correct, there may be a problem with the +10 V reference.
31. Measure voltage at U507B pin 5 while adjusting R561. This is the temperature-compensated adjustable voltage reference to which the detected voltage is compared. It should vary between +0.15 V and +0.6 V.
32. Adjust R561 to its limits and verify that the output U507B pin 7 measures approximately +1 Vdc at one limit and -12 Vdc at the other limit.

### Third LO Driver Amplifier (100 MHz VCXO)

The third LO driver amplifier (Q503) amplifies the 300 MHz from the 300 MHz distribution amplifier to a sufficient level to drive the LO port of the double balanced mixer. During the SIG ID operation, diodes CR501 and CR502 turn off the 3rd LO driver amplifier in order to minimize the amount of 300 MHz going to the double-balanced mixer.

#### Check level at amplifier input (steps 1-6)

1. Press **AUX CTRL**, **INTERNAL MIXER**. Press **SIG ID OFF**, if option 008 is installed.
2. Use an active-probe/spectrum-analyzer combination to confirm the power level of the 300 MHz signal at the following test points:

|               |                |
|---------------|----------------|
| A15X602 pin 5 | $\geq +7$ dBm  |
| A15TP504      | $\geq +15$ dBm |

3. If the signal at A15X602 pin 5 is low, but the signal at A15TP504 is correct, press **AUX CTRL**, **INTERNAL MIXER**. Press **SIG ID OFF**, if present.
4. Check that PIN diode switches CR603 and CR605 are reverse biased by approximately +10 Vdc. Refer to function block F of A15 RF schematic.
5. Measure 300 MHz signal at A15TP503 using an active probe/spectrum analyzer combination. If the signal is not approximately +10 dBm, refer to “Unlocked Reference PLL (100 MHz VCXO)” in this chapter.
6. If the level at the TP503 is correct, but signal at TP504 is too low, the fault is probably in the amplifier.

---

## Unlocked Reference PLL (600 MHz SAWR)

---

**Note** The following information is for A15 RF assemblies earlier than 08563-60054, 08563-60055, or 08563-60056. For A15 RF assemblies with the aforementioned HP part numbers, refer to *Unlocked Reference PLL (100 MHz VCXO)* earlier in this chapter.

---

### Operation (600 MHz SAWR)

The reference PLL's 600 MHz output is generated by a 600 MHz SAWR (surface acoustical wave resonator) VCO. The SAWR provides a high Q feedback path in the oscillator ensuring good phase noise. If the oscillator is off-frequency, the phase-lock circuitry is probably at fault. If there is no signal present at A15J701, or if the level is less than  $-3$  dBm, the oscillator has failed. Transistor Q703 provides active bias for oscillator transistor Q701. Transistor Q704 provides active bias for 600 MHz buffer amplifier Q702. Refer to function blocks Q and R of A15 RF schematic in the *HP 8560E/HP 8561E/HP 8563E Component Level Information* binder.

### Troubleshooting (600 MHz SAWR)

1. If Q701 and Q703 are functioning, check the bias on varactors CR701 and CR702. The varactors should be reverse-biased between 0 V and 18 V, depending on tune voltage.
2. If the active devices are functioning properly, check the SAWR by placing a 100-ohm resistor across U701 pins 1 and 2. This bypasses the SAWR, but provides the equivalent loss of a correctly functioning SAWR.
3. If the oscillator begins to oscillate, the SAWR is probably defective.
4. On the HP 8560E, press **AUX CTRL**, **REAR PANEL**, and **10 MHz INT**.
5. Measuring tune line voltage (LO3 ERR) indicates if the Reference PLL is locked. Measure the voltage at A15J502 pin 3. Connect the ground lead to A15J200 pin 6.
6. If voltage is not between 0 V and 5.75 V the loop is unlocked and **ERR 333 600 UNLK** should be displayed on the CRT.
7. If the 600 MHz oscillator is working, the reason for the unlocked condition is either a problem in the 10 MHz reference or a fault in the signal path around the loop.

#### Check 10 MHz reference to phase/frequency detector (steps 8-13)

8. On the HP 8560E, press **AUX CTRL**, **REAR PANEL**, and **10 MHz INT**.
9. Check the 10 MHz reference frequency-accuracy by connecting a frequency counter to A15J301 and verify that the reference frequency is  $10\text{ MHz} \pm 40\text{ Hz}$  after a 5 minute warm-up period.
10. If a 10 MHz signal  $>1$  V peak-to-peak is not present at A15J301, refer to the "10 MHz Reference" in Chapter 11.
11. Measure the signal on U504 pin 3 with an oscilloscope. Refer to function block O of A15 RF schematic.

12. Measure the signal at U504 pin 11 with an oscilloscope. Refer to function block O of A15 RF schematic. This signal should be TTL levels at 10 MHz with a 90 percent duty cycle.
13. If TTL-level signals (approximately 10 MHz) are not present, check signals backwards through the loop to find a fault in the signal path.
14. Use an oscilloscope to check for 50 MHz TTL level signal at U503 pin 2. Refer to function block X of A15 RF schematic.
15. Measure the signals at the following test points with an active probe/spectrum analyzer combination such as an HP 85024A/HP 8566A/B. The signal level at TP701 should be sufficient to drive an ECL input.

|             |                                           |
|-------------|-------------------------------------------|
| U502 pin 2  | 50 MHz, $\geq +3$ dBm                     |
| U502 pin 15 | 300 MHz, $\geq +3$ dBm                    |
| TP503       | 300 MHz, approximately +8 dBm             |
| TP502       | 300 MHz (ECL level), approximately +3 dBm |
| TP701       | 600 MHz (ECL level), approximately +3 dBm |

16. If an approximately 10 MHz TTL signal is present at U504 pin 11 with 90 percent duty cycle, and the RF portion of the phase-lock loop is functioning, the fault probably lies in the phase/frequency detector or the 600 MHz reference loop amplifier.

#### **Check phase/frequency detector (steps 17-22)**

17. Monitor U504 pins 5 and 9 with an oscilloscope. These are the two outputs of the phase/frequency detector. Refer to function block O of A15 RF schematic.
18. A locked loop will exhibit stable, narrow (approximately 20 ns wide), and positive-going TTL pulses occurring at a 10 MHz rate at U504 pins 5 and 9.
19. If the loop is unlocked, but signals are present on both inputs of the phase/frequency detector, the output pulses will be superimposed on each other.
20. If the loop is unlocked, and there is no signal at one of the phase/frequency detector inputs, one phase detector output will be at TTL low and the other will be at TTL high. For example, if there is no input signal at U504 pin 3, U504 pin 5 will be TTL low and U504 pin 9 will be TTL high. If there is no input signal at U504 pin 11, U504 pin 9 will be TTL low and U504 pin 5 will be TTL high.
21. To remove the 10 MHz reference input to the phase/frequency detector, press **AUX CTRL**, **REAR PANEL**, and **10 MHz EXT** with no signal applied to the rear-panel 10 MHz REF IN/OUT connector.
22. To remove the divided-down 600 MHz signal from the phase/frequency detector, short R572. Refer to function block W of A15 RF schematic.

#### **Check the 600 MHz reference loop amplifier (steps 23-26)**

23. Remove 10 MHz reference input to the phase/frequency detector by pressing **AUX CTRL**, **REAR PANEL**, and **10 MHz EXT**. No signal should be connected to the rear-panel 10 MHz REF IN/OUT connector.

---

**Note** The outputs of phase/frequency detector are low-pass filtered to reduce the 10 MHz component of the signal. The filtered signals are then integrated by U506 and the result is fed to the tune line of the 600 MHz oscillator.

---

24. Check that the voltage on A15J502 pin 3 is less than 0 Vdc. Refer to function block P of A15 RF schematic.
25. Press **AUX CTRL**, **REAR PANEL**, and **10 MHz INT** and remove the divided-down 600 MHz input to the phase/frequency detector by shorting R572.
26. Check that the voltage on A15J502 pin 3 is greater than 5.75 Vdc.
27. Replace C519 in X501.
28. If the loop is locked, the voltage on A15J502 pin 3 should be between 0 V and +5.75 Vdc.
29. If the front-panel CAL OUTPUT amplitude is out of specification and cannot be brought within specification by adjusting A15R561, CAL AMPTD, check the calibrator AGC amplifier with the following steps. Refer to function block W of A15 RF schematic.

---

**Note** The 300 MHz CAL OUTPUT signal comes from the divided down 600 MHz which is passed through a leveling loop. The 300 MHz signal passes through a low-pass filter for reducing higher harmonics. These harmonics can fool the detector. The 300 MHz signal passes through a variable attenuator controlled by PIN diode CR503 which is controlled by the feedback loop. Diode CR504 is the detector diode (the same type as CR505). Diode CR504 provides temperature compensation between the reference voltage and the detected RF voltage.

---

- a. Measure the level of 300 MHz at A15 TP505 with an active probe/spectrum analyzer combination. If the signal is less than +2 dBm, repeat the first 29 steps of this procedure.
  - b. If the signal at this point is correct, place a short across the PIN diode CR503.
  - c. If the signal level at the CAL OUTPUT is still less than -10 dBm with CR503 shorted out, troubleshoot the RF forward path through amplifier Q505. (The signal amplitude decreases.)
  - d. If the CAL OUTPUT signal level is greater than -10 dBm, troubleshoot the PIN diode attenuator, the detector, or the feedback path.
30. Measure the detector voltage at A15J502 pin 14. The voltage should measure approximately +0.3 Vdc when the CAL OUTPUT signal is at -10 dBm. This voltage should change with adjustment of A15R561, CAL AMPTD.
  31. Check that the voltage at U507A Pin 3 is +1.7 Vdc. If this voltage is not correct, there may be a problem with the +10 V reference.
  32. Measure voltage at U507B pin 5 while adjusting R561. This is the temperature-compensated adjustable voltage reference to which the detected voltage is compared. It should vary between +0.15 V and +0.6 V.
  33. Adjust R561 to its limits and verify that the output U507B pin 7 measures approximately +1 Vdc at one limit and -12 Vdc at the other limit.

### Third LO driver amplifier (600 MHz SAWR)

The third LO driver amplifier (Q503) amplifies the 300 MHz from the 600 MHz phase-lock loop to a sufficient level to drive the LO port of the double balanced mixer. During the SIG ID operation, (Option 008 only), diodes CR501 and CR502 turn off the 3rd LO driver amplifier in order to minimize the amount of 300 MHz going to the double-balanced mixer.

#### Check level at amplifier input (steps 1-6)

1. Press **AUX CTRL**, **INTERNAL MIXER**. For Option 008, press **SIG ID OFF**.
2. Use an active-probe/spectrum-analyzer combination to confirm the power level of the 300 MHz signal at the following test points:

|          |                |
|----------|----------------|
| A15TP602 | $\geq +7$ dBm  |
| A15TP504 | $\geq +15$ dBm |
3. If the signal at A15TP602 is low, but the signal at A15TP504 is correct, press **AUX CTRL**, **INTERNAL MIXER**. For Option 008, press **SIG ID OFF**.
4. Check that PIN diode switches CR603 and CR605 are reverse biased by approximately +10 Vdc. Refer to function block F of A15 RF schematic.
5. Measure 300 MHz signal at A15TP503 using an active probe/spectrum analyzer combination. If the signal is not approximately +10 dBm, refer to "Unlocked Reference PLL (600 MHz SAWR)" in this chapter.
6. If the level at the TP503 is correct, but signal at TP504 is too low, the fault is probably in the amplifier.

---

## Unlocked Offset Lock Loop (Sampling Oscillator)

### Operation

The offset lock loop drives the A15U100 sampler. The offset lock loop's sampling oscillator tunes to one of sixteen discrete frequencies between 285 MHz and 297.222 MHz. Refer to A15 schematic. Mixer A15U400 mixes the oscillator's output with 300 MHz from the reference PLL, producing a 3 MHz to 15 MHz IF signal. The 3 MHz to 15 MHz signal is compared in the phase/frequency detector with the divided-down 300 MHz from the reference PLL. The phase/frequency detector drives a voltage-to-current diode switch which drives the loop integrator. Loop bandwidth switches vary the loop bandwidth to minimize noise sidebands. The sampling oscillator must produce low noise because the A15U100 sampler multiplies noise by a factor of approximately 24.

Table 10-6 lists the prescaler and postscaler divide numbers in the offset loop reference divide chain, for each of the 16 discrete frequencies to which the offset lock loop may be set. It also indicates what the reference frequency into the phase/frequency divide chain is. Refer to function block AN on the RF schematic.

### Troubleshooting

#### Check loop references (steps 1 and 2)

1. Use an active probe and spectrum analyzer to confirm the presence of the following reference to the offset lock loop's input.

A15TP404

300 MHz at +5 dBm

2. This signal is not correct, refer to "Unlocked Reference PLL" in this chapter.

#### Check levels into mixer (steps 3-13)

3. Set the HP 8560E to the following settings:

|                  |              |
|------------------|--------------|
| Center frequency | .....300 MHz |
| Span             | ..... 0 Hz   |
| Trigger          | ..... SINGLE |

4. Force the PLL to unlock by shorting A15X201 pin 1 to A15X201 pin 5 with a short length of wire. Then connect a dc power supply to A15J200 pin 16.
5. Monitor A15TP201 with an active probe/spectrum analyzer combination. Vary the dc supply until the frequency of the sampling oscillator is 296 MHz.
6. The voltage required to tune the oscillator should measure between +15 Vdc and +19 Vdc. If the voltage is out of this range, perform the sampling oscillator adjustment in Chapter 2.
7. Vary the voltage to tune the sampling oscillator to 296 MHz.
8. Use an active probe/spectrum analyzer combination to measure the 300 MHz LO signal at the following test point:

A15TP402

+7 dBm

9. If the signal is not measured near the indicated power, troubleshoot the offset lock loop buffer (function block AM of A15 RF schematic sheet 3 of 4).

**Table 10-6. Sampling Oscillator PLL Divide Numbers**

| Sampling Oscillator Frequency (MHz) | Center Frequency* (MHz) | Reference Divide Chain |            | Reference Frequency (MHz) |
|-------------------------------------|-------------------------|------------------------|------------|---------------------------|
|                                     |                         | Prescaler              | Postscaler |                           |
| 285.000                             | 2156.3                  | 10                     | 2          | 15.000                    |
| 286.364                             | 2176.3                  | 11                     | 2          | 13.636                    |
| 287.500                             | 2199.5                  | 8                      | 3          | 12.500                    |
| 288.462                             | 2230.3                  | 13                     | 2          | 11.538                    |
| 288.888                             | 799.3                   | 9                      | 3          | 11.111                    |
| 290.000                             | 2263.3                  | 10                     | 3          | 10.000                    |
| 290.909                             | 2282.3                  | 11                     | 3          | 9.091                     |
| 291.666                             | 2302.3                  | 9                      | 4          | 8.333                     |
| 292.500                             | 2155.3                  | 8                      | 5          | 7.500                     |
| 293.478                             | 2158.3                  | 23                     | 2          | 6.522                     |
| 294.444                             | 2336.3                  | 9                      | 6          | 5.556                     |
| 295.000                             | 2196.3                  | 10                     | 6          | 5.000                     |
| 296.000                             | 1.3                     | 15                     | 5          | 4.000                     |
| 296.471                             | 2378.3                  | 17                     | 5          | 3.529                     |
| 297.000                             | 2410.3                  | 20                     | 5          | 3.000                     |
| 297.222                             | 2422.3                  | 18                     | 6          | 2.778                     |

\* To set the sampling oscillator to a desired frequency, set span to 0 Hz and **CENTER FREQ** to the value listed in the table.

10. Measure the 296 MHz loop feedback signal at the following test point:

A15TP400

+2 dBm

11. If the feedback signal is not near the indicated power, measure the signals at the following test points on the feedback path. Refer to function blocks AD, AG, and AH of A15 RF schematic.

A15TP200

+4 dBm

A15TP201

+9 dBm

A15TP202

+5.5 dBm

12. Measure the 4 MHz loop-IF signal at the mixer output. The frequency of the IF is the same as the reference frequency and can be found in Table 10-6.

A15R447 (end nearest L414)

−6 dBm

13. If the IF signal is not near the indicated power, troubleshoot the loop mixer (function block AI).

**Check path to phase/frequency detector (steps 14-19)**

14. Measure the loop IF signal at the input to the IF amplifier/limiter (function block AK):

A15L428 (end nearest U411)      4 MHz (approximately -6 dBm)

15. Confirm the presence of a 4 MHz square-wave reference frequency signal at U406 pin 3. The square wave is TTL and should go below +0.6 V and above +2.2 V.
16. Disconnect the jumper from X201 pins 1 and 5. Disconnect the dc power supply which is connected to A15J200 pin 16.
17. Set HP 8560E to the following settings:

Center frequency ..... 300 MHz  
Span ..... 0 Hz

18. Use an oscilloscope to confirm the presence of a 4 MHz TTL-level reference frequency signal at U406 pin 11.
19. Connect a short across A15R425. Connect A15U406 pins 3 and 11 together. This puts the same signal on both the phase/frequency detector inputs.
20. Observe the phase/frequency detector outputs, U406 pins 6 and 9, with an oscilloscope. Narrow TTL pulses should be present. Pin 9 is normally low, pulsing high, and pin 6 is normally high, pulsing low.
21. Check the end of L417 (nearest C445) with an oscilloscope. With the oscilloscope's input ac-coupled, a triangle waveform approximately 20 mVp-p should be present.
22. Short C441 with a wire jumper. (Connect the jumper from the end of R462 nearest C441 to the end of R460 nearest C443.) This changes the loop integrator into a voltage follower. Refer to function block AB of A15 RF schematic.
23. Check the voltages at the following points:

|               |                          |
|---------------|--------------------------|
| A15U408 pin 6 | +2.5 Vdc (approximately) |
| A15X201 pin 1 | +2.5 Vdc (approximately) |

24. If the voltages are not correct suspect A15U408.
25. Remove the jumpers.

---

## Unlocked YTO PLL

### Operation

The A11 YTO is locked to two other oscillators, the fractional N oscillator and the offset PLL's sampling oscillator. For LO spans of 2.01 MHz and above, either the FM or main coil of the YTO is swept directly. For LO spans of 2 MHz and below, the fractional N oscillator is swept. The sampling oscillator remains fixed-tuned during all sweeps.

The output of A11 YTO feeds through the A7 LO distribution amplifier (LODA) to the A15U100 sampler. The offset PLL's sampling oscillator, which drives the sampler, oscillates between 285 and 297.222 MHz. The sampler generates harmonics of the sampling oscillator and one of these harmonics mixes with the YTO frequency to generate the sampler IF frequency. As a result, the frequency of the sampler IF is determined by the following equation:

$$F_{IF} = F_{YTO} - (N \times F_{SAMP})$$

Where:

$F_{IF}$  is the sampler IF

$F_{YTO}$  is the YTO's frequency

N is the desired sampling oscillator harmonic

$F_{SAMP}$  is the sampling oscillator frequency

Notice that  $F_{IF}$  can be positive or negative depending upon whether the sampling oscillator harmonic used is below or above the YTO frequency. The actual sampler IF is always positive, but the sign is carried along as a "bookkeeping" function which determines which way to sweep the fractional N oscillator (up or down) and what polarity the YTO error voltage should have (positive or negative) to maintain lock.

To check if a negative sampler IF is selected, press **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, **FRAC N FREQ**. If the fractional N oscillator frequency is positive, the sampler IF is also positive. A negative fractional N frequency indicates that the sampler IF is negative.

Notice that the polarity of the YTO loop error voltage (YTO ERROR) out of the YTO loop phase/frequency detector changes as a function of the polarity of the sampler IF. That is, for positive sampler IFs, an increasing YTO frequency results in an increasing YTO ERROR signal. For negative sampler IFs, an increasing YTO frequency results in a decreasing YTO ERROR signal. This implies that to maintain lock in both cases, the sense of YTO ERROR must be reversed such that, with a negative sampler IF, an increasing YTO ERROR results in an increasing YTO frequency. This is accomplished with error-sign amplifier, A14U328B. This amplifier can be firmware-controlled to operate as either an inverting or non-inverting amplifier. Digital control line ERRSGN (from A14U313 pin 19) controls the polarity of this amplifier. When ERRSGN is high (positive sampler IF), the amplifier has a positive polarity.

In fractional N spans (LO Spans  $\leq 2$  MHz) the YTO remains locked to the sweeping fractional N PLL. Thus, the sampler IF must always equal the fractional N oscillator frequency (conditions for lock). Since the YTO must always sweep up in frequency, for negative sampler IFs, the fractional N oscillator must sweep from a higher frequency to a lower frequency. This is necessary since an increasing YTO frequency decreases the sampler IF for negative sampler IFs. The opposite is true for positive sampler IFs, so in these cases, the fractional N oscillator sweeps more conventionally from a lower frequency to a higher frequency.

Table 10-7 summarizes the amplifier polarities for the various combinations of sampler IF polarities and LO spans.

The YTO main coil filter is used to improve residual FM in FM and fractional N spans. See function block I of A14 frequency control schematic in the Component-Level Information binder. Transistors Q304 and Q305 switch the filter (capacitor C36 and resistor R48) into the circuit. Transistor Q303 and U333 keep C36 charged during main spans so the frequency does not jump when C36 is switch in.

**Table 10-7. Amplifier Polarities**

|                                          |                        | <b>YTO Error<br/>Sign Amplifier</b> | <b>ERRSGN<br/>(A14U313 pin<br/>19)</b> |
|------------------------------------------|------------------------|-------------------------------------|----------------------------------------|
| <b>Fractional N<br/>Oscillator Swept</b> | Positive<br>Sampler IF | Positive                            | TTL High                               |
|                                          | Negative<br>Sampler IF | Negative                            | TTL Low                                |
| <b>FM/Main YTO<br/>Coils Swept</b>       | Positive<br>Sampler IF | Positive                            | TTL High                               |
|                                          | Negative<br>Sampler IF | Negative                            | TTL Low                                |

### **Troubleshooting an unlocked YTO PLL**

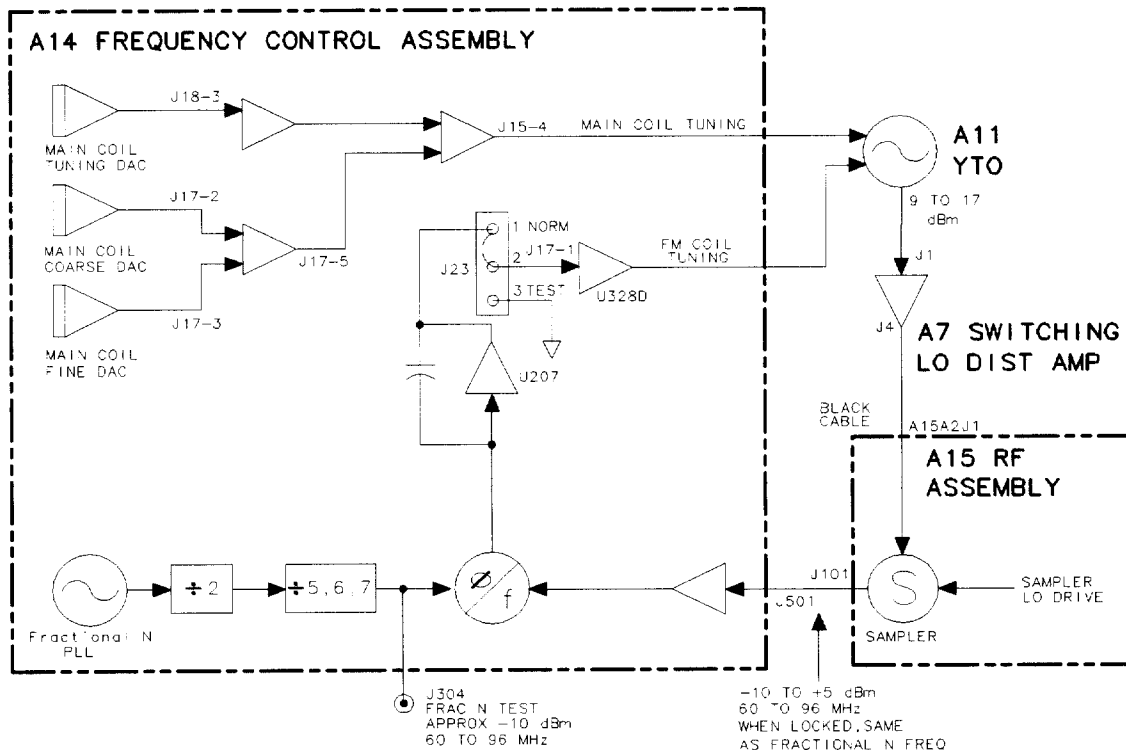
1. If the YTO PLL is unlocked, error code 301 should be displayed. Place the HP 8560E in ZERO SPAN. Figure 10-7 illustrates the simplified YTO PLL.
2. Move the jumper on A14J23 to connect pins 2 and 3 (TEST position). Refer to Figure 10-3 for the location of A14J23. Error code 301 should no longer be displayed. (The YTO PLL's feedback path is now open and the YTO error voltage is forced to zero.)

3. On the HP 8560E, press **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, and **LO FREQ**. The displayed LO FREQ is the desired YTO frequency calculated. Record the YTO's calculated frequency below:

YTO Frequency (calculated) = \_\_\_\_\_GHz

4. Measure the YTO frequency at the front-panel's 1ST LO OUTPUT jack and record below:

YTO Frequency (measured) = \_\_\_\_\_GHz



sp131e

**Figure 10-7. Troubleshooting an Unlocked YTO PLL**

5. Calculate the YTO's frequency error by subtracting the frequency recorded in step 3 from the frequency recorded in step 4. Record the result below:

YTO Frequency Error = \_\_\_\_\_MHz

$$\text{YTO Frequency Error} = \text{YTO Frequency (MEASURED)} - \text{YTO Frequency (CALCULATED)}$$

6. On the HP 8560E, press **MORE 1 OF 2**, **FREQ DIAGNOSE**, and **FRAC N FREQ**. Record the fractional N frequency below:

Fractional N frequency = \_\_\_\_\_MHz

---

**Caution** Replacement of the phase/frequency detector chip A14U204 is not recommended. The part is very delicate and requires special tooling to install successfully.

---

7. If the YTO frequency error recorded in step 5 is greater than 20 MHz, do the following:
  - a. Check the YTO Adjustments using the TAM or the procedure in Chapter 2.
  - b. Check the YTO DACs using the procedure in steps 41 through 49 below, or using manual probe troubleshooting with the TAM on A14J17 and A14J18.
  - c. Refer to steps 9 through 33 below.
8. If the YTO Frequency error recorded in step 5 is less than 20 MHz, do the following:
  - a. Measure the frequency at A14J304. The frequency should be equal to the frequency recorded in step 6. If not, refer to “Unlocked Fractional N PLL” in this chapter.
  - b. Measure the input and output levels of the A15U100 sampler. If the sampler appears defective, check the LO drive to the sampler as described in “Sampler and Sampler IF.”
  - c. Refer to steps 34 through 51 below.

**Check first LO pretune frequency and amplitude (steps 10-13)**

9. The first LO's pretuned frequency must be sufficiently accurate for the YTO loop to acquire lock. The first LO's amplitude must be sufficient to drive the A15U100 sampler. Perform the YTO Adjustment procedure, particularly the YTO main coil adjustments. (If available, use a synthesized microwave spectrum analyzer instead of the microwave frequency counter specified in the adjustment procedure.)
10. If the YTO's main coil cannot be adjusted, proceed to step 33 to troubleshoot the main coil coarse and fine DACs and main coil tune DAC.
11. The front-panel's 1ST LO OUTPUT should measure between +14.5 and +18.5 dBm in amplitude.
12. If the 1ST LO OUTPUT amplitude is out of the specified range, perform the first LO distribution amplifier adjustment procedure. Refer to Chapter 2.

**Check the fractional N oscillator (steps 14-18)**

13. Set the HP 8560E to the following settings:  
Center frequency ..... 300 MHz  
Span ..... 0 Hz
14. Monitor the fractional N PLL's output at A14J304 (FRAC N TEST) with a synthesized spectrum analyzer such as an HP 8568A/B or HP 8566A/B. Refer to function block AI of A14 frequency control schematic.
15. The signal at A14J304 (FRAC N TEST) should measure approximately -10 dBm at 66.7 MHz. If the loop is unlocked, the sampler IF frequency can also be seen on A14J304, about 30 dB below the fractional N signal, when unlocked.
16. If a problem exists only at particular CENTER FREQ and SPAN settings, determine the desired fractional N oscillator frequency by pressing **[CAL]**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, **FRAC N FREQ** and setting the HP 8560E to SINGLE trigger mode.

17. If the fractional N oscillator frequency is not correct, refer to “Unlocked Fractional N PLL” in this chapter.

**Check sampler drive output of A7 LODA (steps 19-22)**

18. Set jumper A14J23 to the TEST position and set the HP 8560E to the following settings:

Center frequency ..... 2.9 GHz  
Span ..... 0 Hz

19. Disconnect cable W34 from A15U100J1.
20. Use a power meter to measure the A7 LODA sampler-drive output at the end of W34. The power should measure greater than  $-9$  dBm.
21. Place jumper A14J23 in the NORMAL position and reconnect W34 to A15U100J1.

**Check sampler IF (steps 23-27)**

22. Set the HP 8560E to the following settings:

Center frequency ..... 300 MHz  
Span ..... 0 Hz

23. Place jumper A14J23 in the TEST position.
24. Disconnect W32 from A15J101. Monitor the sampler IF output (A15J101, SAMPLER IF) with a synthesized spectrum analyzer such as an HP 8568A/B or HP 8566A/B.
25. The sampler IF should measure between 46 MHz and 86 MHz at  $-15$  dBm to  $+2$  dBm. If the signal frequency or amplitude is incorrect, refer to “Unlocked Offset PLL” in this chapter.
26. Set jumper A14J23 in the NORMAL position. Reconnect W32 to A15J101.

**Check FM loop sense (steps 28-34)**

27. Set jumper A14J23 in the TEST position.
28. Set the HP 8560E to the following settings:

Center frequency ..... 300 MHz  
Span ..... 0 Hz

29. Connect an RF signal-generator output to A14J501. Set the signal generator to the following settings:

Frequency ..... 56 MHz  
Amplitude ..... 0 dBm

30. Monitor A14J17 pin 1 with a DVM or oscilloscope. Connect ground to A14J17 pin 6.
31. As the signal generator frequency is increased to 76 MHz, the voltage at A14J17 pin 1 should change from approximately  $+12$  V to  $-12$  V.
32. Set the signal generator to the following settings and repeat step 30.

Frequency ..... 56 MHz  
Amplitude .....  $-15$  dBm

33. If the voltage monitored in step 30 is correct with a 0 dBm output but not with  $-15$  dBm output, suspect the limiting amplifier function block AE.
34. Place jumper A14J23 in the NORMAL position and reconnect W32 to A14J501.

### Check YTO FM coil driver and main loop error voltage driver (steps & 35-40)

35. To troubleshoot the YTO FM coil driver, refer to step 6 of "First-LO Span Problems (2.01 MHz to 20 MHz)."
36. Steps 36 through 40 verify that the YTO-loop error voltage is reaching the FM coil. The main loop error voltage driver has a gain of either 1.5 or 15; the spectrum analyzer's firmware controls the gain during the locking process. The error voltage is read by the ADC on the A3 interface assembly. A14U326D calibrates out any offsets from true ground. A14U326A inverts the sense of the YTO loop to lock the YTO on lower sampler-sidebands (YTO frequency < (sampler frequency × sampler harmonic)). The fractional N frequency indicated in the **FREQ DIAGNOSE** menu will be negative when locking to lower sidebands. Refer to function blocks E, M, and N of A14 frequency control schematic in the *HP 8560E/HP 8561E/HP 8563E Component Level Information* binder.

Set the HP 8560E to the following settings:

Center frequency ..... 300 MHz  
Span ..... 0 Hz

37. Remove jumper A14J23 and connect a dc power supply to A14J23 pin 2. Connect ground to A14J23 pin 3. Set the dc power supply to +7.5 Vdc.
38. Verify the nominal test-point voltages listed in Table 10-8.
39. Change the input voltage to -7.5 volts and re-verify that the voltages listed in Table 10-8 are the same except for a change in polarity.
40. Change the **CENTER FREQ** to 678.8 MHz with the **SPAN** remaining 0 Hz. This will change the switch setting of U326A and invert the voltages listed in Table 10-8.

**Table 10-8. Voltages in FM Coil and Main Loop Drivers**

| Measurement Points | Voltages |
|--------------------|----------|
| A14U405 pin 6      | +2.8 Vdc |
| A14U322 pin 2      | 0 Vdc    |
| A14J17 pin 4       | >+10 Vdc |

### Check main coil coarse and fine DAC's (steps 41-44)

41. The main coil coarse and fine DACs correct any initial pretune errors in the YTO main coil. The DACs adjust the FM-coil current to zero before any sweep begins. Refer to function block J of A14 frequency control schematic.
42. Set the HP 8560E to the settings listed below. This sets both DACs to 128 (the DAC setting range is 0 to 255).

Center frequency ..... 300 MHz  
Span ..... 0 Hz  
Trigger ..... SINGLE, EXT  
(with no external trigger connected)

43. Press **SAVE**, **PWR ON STATE** and turn off the spectrum analyzer.
44. Place jumper A14J23 in the TEST position and turn on the spectrum analyzer.

**Check main coil tune DAC (steps 45-49)**

45. Verify the voltages listed in Table 10-9.

**Table 10-9. Main Coil Coarse and Fine DACs Voltages**

| Measurement Points | Voltages |
|--------------------|----------|
| A14J17 pin 2       | –5 Vdc   |
| A14J17 pin 3       | –5 Vdc   |
| A14J17 pin 5       | +5Vdc    |

46. Place jumper A14J23 in the NORMAL position.
47. Set the HP 8560E to the following settings:
 

|                  |              |
|------------------|--------------|
| Center frequency | .....300 MHz |
| Span             | ..... 0 Hz   |
48. Place jumper A14J23 in the TEST position.
49. Measure the output of the main coil tune DAC (A14J18 pin 3) with a DVM. Refer to function block E of A14 frequency control schematic.
50. If the HP 8560E's center frequency is 300 MHz, the voltage at A14J18 pin 3 should measure  $-3.35\text{ V} \pm 0.25\text{ V}$ . The voltage may also be determined from the following equation:
 
$$V = -(\text{First LO Frequency} - 2.95\text{ GHz}) \times 2.654\text{ V/GHz}$$
51. The voltage at A14U330 pin 2 should measure  $-3.4\text{ V} \pm 0.2\text{ Vdc}$ . This represents a current setting the YTO to approximately 2.95 GHz.
52. Return jumper A14J23 to the NORMAL position.

---

## Unlocked Fractional N PLL

### Operation

The fractional N oscillator is used in the HP 8560E as a reference for the first LO phase locked loop. It provides the 1 Hz start- frequency resolution for the first LO, and is the means by which the first LO is swept in LO spans of 2 MHz or less (fractional N spans). The prescaler, fractional N divider, and the postscaler are preset at power-on.

The PLL operates to produce an output frequency in the range of 60 MHz to 96 MHz selectable in 1 Hz increments. The output frequency can be swept (increasing or decreasing) over a selectable 100 Hz to 2 MHz range.

To determine the fractional N frequency for any given center frequency, press **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, and **FRAC N FREQ**. The FRAC N FREQ frequency displayed is the frequency that will be measured at A14J304 with the HP 8560E in zero span.

### Confirming an unlocked condition

1. Set the HP 8560E to the following settings:

Center frequency ..... 300 MHz  
Span ..... 0 Hz

2. Connect A14J304 FRAC N TEST to the input of a synthesized spectrum analyzer and view the fractional N PLL output at 66.7 MHz.

---

|             |                                                                                                                                                                                                            |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note</b> | If a synthesized spectrum analyzer is not available, connect A14J304 to the input of a 20 dB gain amplifier, such as an HP 8447E. Connect the output of the amplifier to the input of a frequency counter. |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

---

3. If the fractional N oscillator measures a stable 66.7 MHz, the fractional N PLL is probably locked.
4. Check the two LED's visible through the shield on A14. If either LED is lit, the fractional N PLL is not locked.
5. If either LED on A14 is lit, and no error message is displayed, check FC MUX A14U305. Refer to function block AH of A14 frequency control schematic.
6. If neither LED is lit, but the output frequency is wrong by more than 1 MHz, check the postscaler, function block AV.
7. Check that the postscaler is dividing properly. The frequency at A14J304 should be equal to the frequency at A14TP4 divided by either 5, 6, or 7. Refer to Table 10-10. To keep the divide number at a constant value set the spectrum analyzer to:

Span ..... 0 Hz  
Trigger ..... SINGLE, EXT  
(with no external trigger connected)

**Table 10-10. Postscaler Divide Numbers**

| Divide Number | D11 | D10 | D9 | Input Range (MHz)<br>(A14J304) | Output Range (MHz)<br>(A14TP4) |
|---------------|-----|-----|----|--------------------------------|--------------------------------|
| 7             | 0   | 0   | 1  | 840 to 973                     | 60.0 to 69.5                   |
| 6             | 0   | 1   | 0  | 834 to 987.96                  | 69.5 to 82.33                  |
| 5             | 0   | 1   | 1  | 823.2 to 960                   | 82.33 to 96.0                  |

If the output frequency is wrong by less than 1 MHz, the phase locked loop is not unlocked but still requires repair. Continue with the “Fractional N Oscillator PLL” section.

### Fractional N PLL

The fractional N PLL provides a synthesized frequency in the range of 60 MHz to 96 MHz. The 800 MHz to 1020 MHz voltage controlled oscillator (VCO) in the loop is divided down to lock with the 2.5 MHz reference. Simultaneously, the VCO is divided by two and then by either 5, 6, or 7 to generate the 60 MHz to 96 MHz output.

The prescaler (function block AR) supplies the clock signal for the fractional divider and is required for the fractional divider to operate. At the start of a fractional N sweep the fractional divider is set to a value for the start frequency and a sweep rate. It then sweeps for as long as HSCAN is high. Use the following procedure to troubleshoot unlocked loop problems or problems of locking to the wrong frequency (by less than 1 MHz):

1. Check the two LEDs on A14 frequency control assembly. If either LED is lit, the fractional N phase locked loop is not locked.
2. The 10 MHz reference is required for fractional N operation. It is divided by four to 2.5 MHz in the reference divider circuitry, block AN. It is used to lock the divided voltage controlled oscillator (VCO) frequency. Check that the 10 MHz reference is present at A14J301. The 10 MHz reference is derived from the 600 MHz reference on the A15 RF assembly.
3. Change the spectrum analyzer from the fractional N span to 0 Hz.
4. Check the frequency at A14TP1. It should equal the value found by pressing **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, and **RAW OSC FREQ**.
5. Check the tune voltage at the ungrounded end of C135.
6. Look up the expected problem area in Table 10-11 with the information from steps 4 and 5. Go to the appropriate troubleshooting steps.

**Table 10-11. Unlocked Fractional N Troubleshooting Areas**

| Measured VCO Frequency Relative to Expected Value | Tune Voltage  |                       |                       |                       |               |
|---------------------------------------------------|---------------|-----------------------|-----------------------|-----------------------|---------------|
|                                                   | Below -12.5 V | About -11 V           | Between $\pm 10$ V    | About +11 V           | Above +12.5 V |
| Measured > expected                               | VCO clamp     | VCO                   | Divider or integrator | Divider or integrator | VCO clamp     |
| Measured < expected                               | VCO clamp     | Divider or integrator | Divider or integrator | VCO                   | VCO clamp     |
| Measured, not oscillating                         | VCO clamp     | VCO                   | VCO                   | VCO                   | VCO clamp     |

7. VCO clamp troubleshooting:

Q131, Q132 and the associated components should limit the tune voltage at R240 to about  $\pm 11$  V. If the integrator (its output voltage is on TP13) tries to produce a voltage outside this range, excess current is shunted through CR131 and Q131 for positive excursions or CR132 and Q132 for negative excursions. The bases of these transistors should be at about  $\pm 9.6$  V for proper operation.

8. VCO troubleshooting:

Check the dc biases in the VCO function block. The bias voltages, for some points in the VCO, are indicated in Figure 10-8.

sp140e

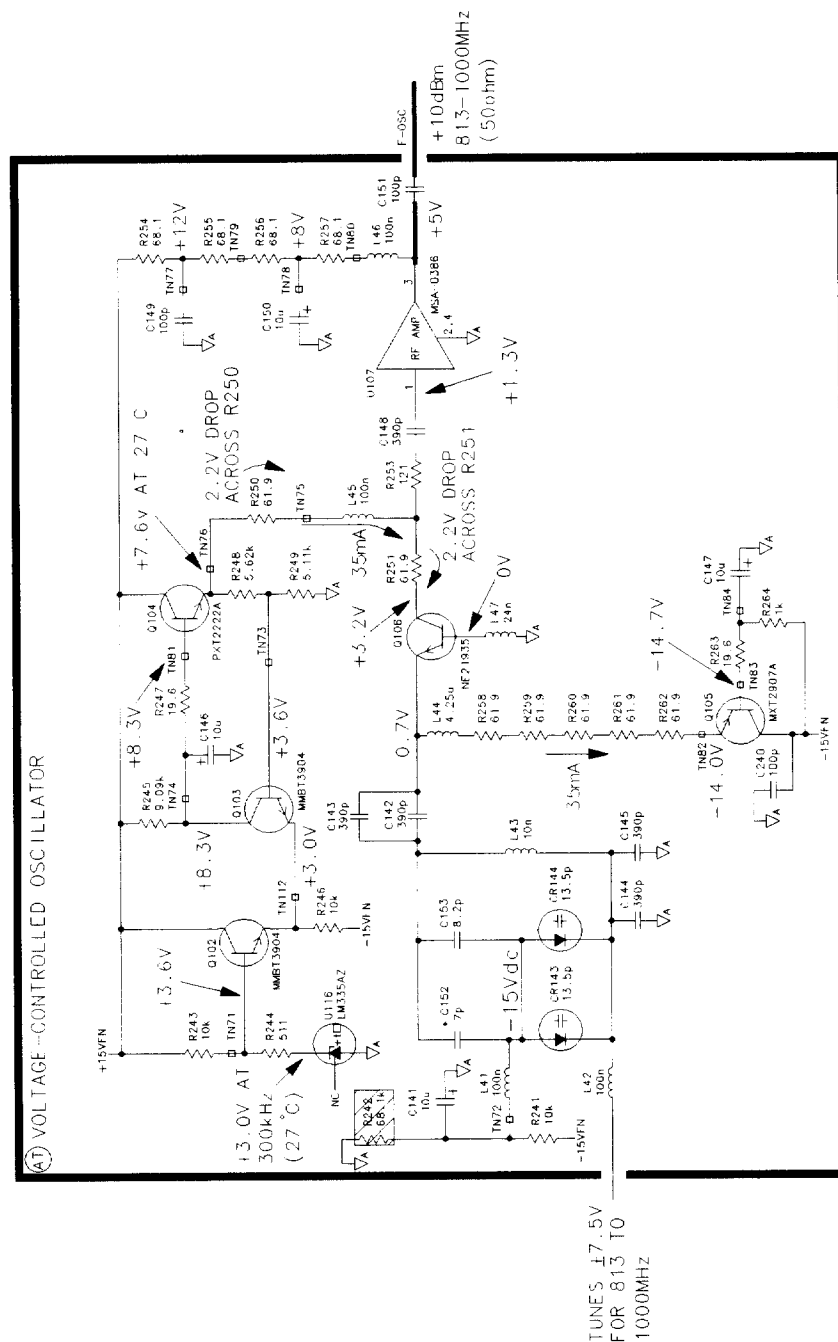


Figure 10-8. VCO Bias Voltages

### 9. Divider and integrator troubleshooting:

Measure the frequency of the pulses at TP6 in block AO. Look up the expected problem area in Table 10-12 and go to the appropriate troubleshooting steps.

**Table 10-12. Divider and Integrator Troubleshooting**

| Measured VCO<br>Frequency Relative<br>to Expected Value | TP6 Frequency |                   |          |                   |
|---------------------------------------------------------|---------------|-------------------|----------|-------------------|
|                                                         | zero          | <2.5 MHz          | 2.5 MHz  | >2.5 MHz          |
| Measured > expected                                     | Dividers      | Dividers          | Dividers | Det or integrator |
| Measured < expected                                     | Both          | Det or integrator | Dividers | Dividers          |

10. Divider troubleshooting:

- Check the frequency at A14TP2. It should be equal to the frequency at A14TP1 divided by two.
- The signal at A14TP3 should be above  $-14$  dBm.
- Use an analog oscilloscope to view the signal at A14TP5. Adjust the scope's triggering to view the divide-by-16 signal. The frequency at this point will be varying as the prescaler changes its divide number to either 16, 17, 20, or 21. The prescaler uses 16 as the divide number most frequently. The frequency displayed on the oscilloscope should equal the frequency from TP2 divided by 16.
- Use an oscilloscope to view the signal at pin 8 of U112. Its average frequency should be given by:

$f = f(\text{A14TP5}) \times 80 \text{ MHz/RAW OSC FREQ}$  where:  $f(\text{A14TP5})$  is the frequency measured at TP5, and RAW OSC FREQ comes from step 4.

If the frequency is in error, the fractional divider, block AS, is not functioning. Check that FRAC N RUN on U113 pin 39 is high.

- Use an oscilloscope to verify that the signals at N\_in (U112 pin 8) and N\_out (TP6) are identical except for a sub-microsecond delay.

Detector and integrator troubleshooting:

Check the phase detector output on TP11 in block AO. If  $F_{\text{ref}}$  is higher in frequency than TP6 (reclocked VCO/N), then the average voltage at TP11 should be positive by 0.05 V to 10 V. If  $F_{\text{ref}}$  is lower, TP11 should be  $-0.05$  V to  $-10$  V.

The polarity of the output of the loop gain (block AP, TP12) should be the same as the polarity of the input (TP11).

The integrator op amp (U106) output (TP13) should try to go very positive (about +12 V) if its average input (TP12) is positive. If its average input is negative, it should try to go very negative (about  $-12$  V). If its average input is zero and it is functioning correctly, it may take on any output voltage between  $-12$  V and +12 V.

## Frequency Span Accuracy Problems

The HP 8560E employs lock-and-roll tuning to sweep the first LO for spans greater than 2.0 MHz. The first LO is locked to the start frequency immediately after the previous sweep has been completed. The first LO is then unlocked, and, when a trigger signal is detected, the first LO sweeps (rolls).

When there is a considerable delay between the end of one sweep and the beginning of the next, the actual first LO start frequency may differ from the locked start frequency. This start frequency drift will be most noticeable in a 2.01 MHz LO span (the narrowest FM coil span). This drift is not noticeable in either free run or line trigger modes. The sweep is generated by different oscillators in the synthesizer section depending on the desired first-LO's span (due to harmonic mixing, this is not necessarily the same as the span setting of the spectrum analyzer). Refer to Table 10-13 for a listing of sweep-signal destinations versus First LO spans. Sweeping the fractional N oscillator results in sweeping the YTO's FM coil. There is a one-to-one relationship between the fractional N oscillator's frequency span and the first-LO's span. The fractional N oscillator sweep is generated digitally. The oscillator is always synthesized, rather than employing lock and roll tuning.

**Table 10-13. Sweep Signal Destination versus Span**

| First LO Span      | Sweep Signal Destination                                               |
|--------------------|------------------------------------------------------------------------|
| >20 MHz            | A11 YTO's main coil                                                    |
| 2.01 MHz to 20 MHz | A11 YTO's FM coil                                                      |
| ≤2 MHz             | None<br>Fractional N oscillator sweeps<br>without a sweep ramp signal. |

### Determining the first LO span

The first-LO's span depends on the spectrum analyzer's harmonic-mixing number. Use the following steps to determine the first LO's span:

1. Read the span setting displayed on the HP 8560E.
2. Determine the harmonic-mixing number from the information in Table 10-14.

**Table 10-14. Harmonic Mixing Number versus Center Frequency**

| Center Frequency  | Harmonic Mixing Number                                      |
|-------------------|-------------------------------------------------------------|
| 1 kHz to 2.9 GHz  | 1                                                           |
| 18 GHz to 325 GHz | 6 through 52<br>depending upon<br>lock harmonic<br>selected |

3. Use the following equation to determine the first LO span used.

$$\text{First LO Span} = \frac{\text{Display's Span Setting}}{\text{Current Band's Harmonic Mixing Number}}$$

4. Refer to Table 10-13 to determine the circuit associated with the span.

### Confirming span problems

1. If all first LO spans or only first-LO spans of 2.01 MHz or above are affected, perform the YTO Adjustment procedure in Chapter 2.
  - a. On the HP 8560E press **CAL**, **REALIGN LO & IF**, and retest all spans.
  - b. If the YTO adjustment has sufficient range and only LO spans of 2.01 MHz or above are faulty, test YTO linearity by performing step c.
  - c. Test the span in question at different center frequencies in the same band. If the span accuracy changes significantly (2% or more), suspect the A11 YTO.
2. If only first-LO spans of 2 MHz or less are faulty, suspect A14's fractional N PLL.
3. If there are several spans in the main coil and FM coil ranges affected, suspect A14's span attenuator.

## YTO main coil span problems (LO spans >20 MHz)

For YTO main coil spans, the YTO is locked at the beginning of the sweep and the sweep ramp is summed into the main coil tune driver.

1. Perform the YTO adjustment procedure in Chapter 2. If the YTO adjustments cannot be performed, continue with step 2.
2. Set the HP 8560E to the following settings:

Start frequency ..... 10 MHz  
Stop frequency ..... 2.9 GHz

3. Verify that a  $-1.2$  V to  $-4.8$  V ramp (approximately) is present at A14U331 pin 2.
4. If this ramp is not present, troubleshoot the main/FM sweep switch. See function block H of A14 frequency control schematic.
5. Measure the output of the main coil tune DAC at A14J18 pin 3. At the frequency settings of step 2, this should be  $-2.48$  V.

If the voltage is not  $-2.48$  V, troubleshoot the main coil tune DAC. See function block E of A14 frequency control schematic.

## YTO FM coil span problems (LO spans 2.01 MHz to 20 MHz)

In YTO FM coil spans, the YTO loop is locked and then opened while the sweep ramp is summed into the FM coil. The FM coil sensitivity is corrected by changing the sensitivity of the FM coil driver.

1. Perform the YTO Adjustment procedure in Chapter 2. If the YTO adjustments cannot be performed, continue with this procedure.
2. Set the HP 8560E to the following settings:

Center frequency ..... 300 MHz  
Span ..... 20 MHz  
Sweep time ..... 50 ms

3. Check for the presence of a 0 V to  $-10$  V sweep ramp at A14J15 pin 14 (input to the main/FM sweep switch). Refer to function block H of A14 frequency control schematic.
4. Check for the presence of a 0 V to  $+5$  V sweep ramp at A14U405 pin 6 (YTO FM coil driver). Refer to function block M of A14 frequency control schematic.
5. Check the state of the Main/FM sweep switches as indicated in Table 10-15.
6. The rest of the procedure troubleshoots the YTO FM coil driver.

Refer to function block M of A14 frequency control schematic.

**Table 10-15. Settings of Sweep Switches**

| Switch | Switch State | Switch Control Line<br>(Pin #) | Control Line State<br>(TTL) |
|--------|--------------|--------------------------------|-----------------------------|
| U318A  | Closed       | 1                              | High                        |
| U318B  | Open         | 16                             | High                        |
| U318C  | Closed       | 9                              | Low                         |
| U318D  | Open         | 8                              | Low                         |

7. Set the HP 8560E to the following settings:

Center frequency ..... 300 MHz  
Span ..... 0 Hz  
Trigger ..... SINGLE, EXT

- a. On the HP 8560E press **SAVE**, **SAVE STATE**, **STATE 0**.
- b. Remove jumper A14J23 and connect a dc voltage source to A14J23 pin 2. Connect the voltage source ground to A14J23 pin 3.
- c. Connect a microwave frequency-counter or spectrum analyzer to the HP 8560E's 1ST LO OUTPUT. (front panel output)
- d. Set the dc-voltage source's output for 0 Vdc and note the 1st LO frequency.
- e. Set the dc-voltage source's output for +10 Vdc. The first LO frequency should momentarily increase approximately +15.6 MHz.
- f. The voltage at A14U332 pin 2 should be approximately 19% of the voltage at A14J23 pin 2.
- g. If the first LO frequency did not change in step e, set the HP 8560E's **LINE** switch off and disconnect W10 from A14J3.
- h. Place a jumper between A14J3 pins 9 and 10. Place a 50  $\Omega$ , 3 watt resistor across A14J3 pins 5 and 6 (resistor, HP part number 0811-1086). Set the **LINE** switch on.
- i. On the HP 8560E, press **RECALL**, **STATE**, **STATE 0**.
- j. The voltage at A14U332 pin 2 should be approximately 19% of the voltage at A14J23 pin 2.
- k. If the voltage at U332 pin 2 is correct with A14J3 pins 9 and 10 shorted, but was incorrect with W10 connected, the YTO FM coil is probably open; replace the A11 YTO.
- l. Replace jumper A14J23. Remove the jumper and resistor from A14J3. Reconnect W10 to A14J3.

### Fractional N span problems (LO spans $\leq 2$ MHz)

If the fractional N spans are inaccurate or nonexistent, but the fractional N PLL is locked to the correct frequency and other spans are correct, there may be a problem with the HSCAN signal. Check that HSCAN is present at the fractional divider, U113 pin 41 in function block AS. HSCAN comes from the A3 interface assembly and goes to the sweep generator circuitry in function block A and to Fractional N.

## First LO span problems (all spans)

1. Set the HP 8560E to the following settings:

|                  |         |
|------------------|---------|
| Center frequency | 300 MHz |
| Span             | 2 MHz   |
| Resolution BW    | 1 MHz   |
| Video BW         | 1 MHz   |
| Sweep time       | 50 ms   |

2. Check that there is 0 V to +10 V ramp of 50 ms duration at A14J15 pin 15.
3. If a scan ramp is not present, refer to "Sweep Generator" in this chapter.
4. If there is a 0 to -10 V ramp at A14J15 pin 14, the fault is probably in the Main/FM sweep switch. See function block H of A14 frequency control schematic.
5. Check that there is a 0 V to +10 V ramp at U325 pin 1. The spectrum analyzer's ADC obtains information about the sweep from this node.

### Check span attenuator (steps 6-13)

6. Continue with step 7 to check the span attenuator. See function block L of A14 frequency control schematic.
7. With the spectrum analyzer set to the settings in step 1, monitor A14U323 pin 6 with an oscilloscope. A 0 V to -10 V ramp should be present.
8. Change the HP 8560E's span to 1 MHz and check for a 0 V to -5 V ramp at U323 pin 6.
9. Change the HP 8560E's span to 400 kHz and check for a 0 V to -2 V ramp at U323 pin 6.
10. Set the HP 8560E to the following settings:

|                 |         |
|-----------------|---------|
| Start frequency | 10 MHz  |
| Stop frequency  | 2.9 GHz |
| Sweep time      | 80 ms   |

11. Monitor A14J15 pin 14 for a 0 V to -7.5 V ramp. Switches U317A, U317B, and U317D should be open and U317C should be closed.
12. Change the HP 8560E's SPAN to 365 MHz and check for a 0 mv to -1.0 V ramp at A14J15 pin 14. Switch U317C should be open and U317B closed.
13. Change the HP 8560E's SPAN to 36.5 MHz and check for a 0 mV to -100 mV ramp at A14J15 pin 14. Switch U317B should be open and U317A closed.

### Check current source (steps 14-21)

14. Check the sweep generator's current source with the following steps (function block A of A14 frequency control schematic).
15. Set the HP 8560E to the following settings:

|                  |         |
|------------------|---------|
| Center frequency | 300 MHz |
| Span             | 1 MHz   |
| Sweep time       | 50 ms   |

16. Use a DVM to monitor the voltage at A14J18 pin 4. The voltage should measure approximately -8.45 Vdc.

17. Set the HP 8560E's sweep time to 100 ms. The voltage at J18 pin 4 should measure approximately  $-4.21$  Vdc.
18. Set the HP 8560E's sweep time to 200 ms. The voltage at J18 pin 4 should measure approximately  $-2.1$  Vdc.
19. The analog switches and comparators should be set as listed in Table 10-16.
20. Check that U312D opens when the sweep time is set to 2 seconds.
21. Check that U312B and U312C close when the sweep time is set to 20 seconds.

**Table 10-16. Settings for Switches and Comparators**

| Sweep Time | Switch<br>U312B | Switch<br>U312C | Switch<br>U312D | Comparator<br>U319A Pin 1 | Comparator<br>U319B Pin 7 |
|------------|-----------------|-----------------|-----------------|---------------------------|---------------------------|
| 200 ms     | Open            | Open            | Closed          | High                      | High                      |
| 2 s        | Open            | Open            | Open            | High                      | High                      |
| 20 s       | Closed          | Closed          | Open            | High                      | High                      |

---

## Phase Noise Problems

System phase noise can be a result of noise generated in many different areas of the spectrum analyzer. When the spectrum analyzer is functioning correctly, the noise can be observed as a function of the distance away (the offset) from the carrier frequency. The major contributor to system noise can be characterized as coming from specific circuit areas depending upon the offset frequency.

Some very general recommendations can be made for identifying which circuitry is the cause of the noise at certain offsets. The recommendations below apply with a center frequency of 1 GHz.

| Carrier Frequency Offset | Major Contributor (when working correctly) |
|--------------------------|--------------------------------------------|
| 100 Hz                   | Reference (OCXO or TCXO)                   |
| 1 kHz                    | 600 MHz reference PLL                      |
| 3 kHz                    | Fractional N PLL                           |
| 10 kHz to 150 kHz        | Offset lock loop or YTO loop               |
| >150 kHz                 | YTO                                        |

### Phase noise in locked versus lock and roll spans

Input a signal to the spectrum analyzer. Set the center frequency to the input signal frequency, set the span to 2 MHz, and plot the display. This plots the system noise for a locked sweep. Plot the display again with a span of 2.01 MHz (lock and roll sweep). The crossover point of the noise floor of the two plots is typically at an offset of about 50 kHz, for a functioning instrument.

If the crossover point is shifted out to a higher offset frequency, suspect the YTO loop circuitry.

If the crossover point is shifted in to a lower offset frequency, suspect the offset or fractional N loop circuitry.

### Reference versus reference PLL phase noise

If the problem seems to be in the frequency reference or reference PLL circuitry, measure the noise with internal and external references. If there is no difference, suspect the circuitry associated with the SAWR A15U701. If there is a difference, look at 10 MHz distribution, OCXO, or TCXO.

### **Fractional N versus offset PLL or YTO PLL phase noise**

If the spectrum analyzer has excessive noise at  $>1$  kHz offset, measure the noise with center frequencies of 100 MHz and 2.5 GHz.

If the measurements are equal, suspect the fractional N circuitry and the YTO loop circuitry on the A14 frequency control assembly.

If the measurements differ by 2 dB to 5 dB, with the 2.5 GHz measurement at a higher noise level, suspect the offset lock loop circuitry.

### **Fractional N PLL phase noise**

Check the noise on the 5 V regulators on A14, particularly the regulator in the reference divider circuitry A14U121. Refer to function block AN on the A14 frequency control assembly schematic.

The noise level of the voltage regulator should be  $<1$  mV. The typical noise level is  $40\ \mu\text{V}$  RMS between 10 Hz and 100 kHz.

A coaxial probe with very little unshielded tip area should be used to avoid picking up radiated 60 Hz. Check that your measurement is valid by probing ground on the circuit and verifying that the measured value is well under the 1 mV threshold that indicates a defective regulator.

There can also be phase noise problems if the loop gain is incorrect. See function block AP for loop gain troubleshooting information.

## Sampler and Sampler IF

The A15U100 sampler creates and mixes harmonics of the sampling oscillator with the first LO. The resulting sampler IF (60 MHz to 96 MHz) is used to phase-lock the YTO. The sampler IF filters unwanted products from A15U100's output and amplifies the IF to a level sufficient to drive the YTO loop. When the IF is less than 87.14 MHz, PIN diodes switch a 120 MHz low pass filter in the sampler IF section.

1. Set HP 8560E to the following settings:

Center frequency ..... 300 MHz  
Span ..... 0 Hz

2. Disconnect W32 from A15J101.

3. Connect the input of a power splitter to A15J101. Connect W32 to one of the splitter outputs. Connect the other splitter output to the input of another spectrum analyzer.

4. If a 66.7 MHz signal, greater than  $-15$  dBm, is not displayed on the other spectrum analyzer, set a microwave source to the following settings:

Frequency ..... 4.2107 GHz  
Amplitude .....  $-5$  dBm

5. Connect the microwave source to A15U100J1. A 66.7 MHz signal at approximately 0 dBm should be displayed on the other spectrum analyzer.

6. Use an active probe/spectrum analyzer combination to measure the signal at the following test points:

|          |                    |
|----------|--------------------|
| A15TP101 | 66.7 MHz, $-8$ dBm |
| A15TP201 | 296 MHz, $+9$ dBm  |

7. If a correct signal is seen at A15TP201 but the signal at A15TP101 is wrong, proceed as follows:

Use an oscilloscope to measure the signals at the following test points:

|               |                                                       |
|---------------|-------------------------------------------------------|
| A15J400 pin 1 | $+0.8$ Vdc to $+1.6$ Vdc ( $\leq 0.5$ Vp-p variation) |
| A15J400 pin 3 | $-0.8$ Vdc to $-1.6$ Vdc ( $\leq 0.5$ Vp-p variation) |

If these levels are wrong, perform the "Power and Sampler Match Adjustments" in the sampler oscillator adjustment procedure. Refer to Chapter 2.

If adjusting the sampler match does not bring the signal at A15TP101 within specification when the signal at A15TP201 is correct, the A15U100 sampler is defective.

8. The sampler IF signal at A15J101 is 60 MHz to 96 MHz at  $-10$  dBm to  $+5$  dBm. If the signal at A15TP101 is correct, but the signal at A15J101 is wrong, the fault lies in the sampler IF circuitry. Continue with the following steps.

9. Set the HP 8560E to the following settings:

Center frequency ..... 300 MHz  
Span ..... 0 Hz

10. Set a microwave source to the following settings:
 

|                 |            |
|-----------------|------------|
| Frequency ..... | 4.2107 GHz |
| Amplitude ..... | −5 dBm     |
11. Connect the microwave source to A15U100J1.
12. Measure the signal at U103 pin 1 using an active probe/spectrum analyzer combination.
13. If a 94.7 MHz signal, approximately −14 dBm, is present, but the signal at A15J101 is low, suspect U103.
14. When U104 pin 3 is at TTL low, U104 pin 6 should near −15 Vdc and PIN diodes CR101, CR102, and CR103 should be reverse-biased.
15. Set HP 8560E to the following settings:
 

|                        |          |
|------------------------|----------|
| Center frequency ..... | 89.3 MHz |
| Span .....             | 0 Hz     |
16. Check that U104 pin 3 is at a TTL high and U104 pin 6 is greater than +7 V. PIN diodes CR101, CR102, and CR103 should all be turned on with about 7 mA of forward current.
17. Disconnect the power splitter and reconnect W32 to A15J101.

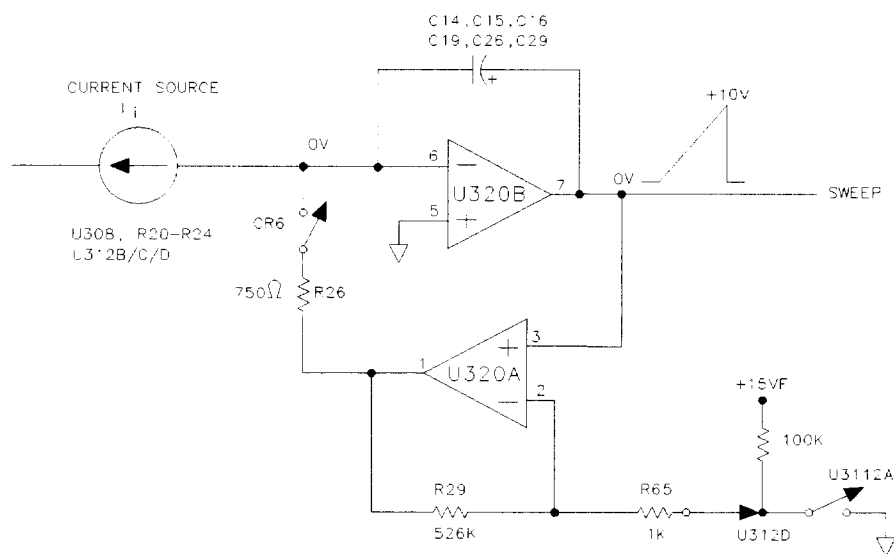
---

## Sweep Generator Circuit (for Spectrum Analyzers with 100 s max. Sweep Time)

The sweep generator operates by feeding a constant current from DAC U307 into an integrator, U320B. See function block A of A14 frequency control schematic. This current is scaled by resistors R20 through R24 and U312B/C/D. See Figure 10-9. The capacitors used in the integrator depend on the sweeptime range; smaller-value capacitors provide faster sweep times.

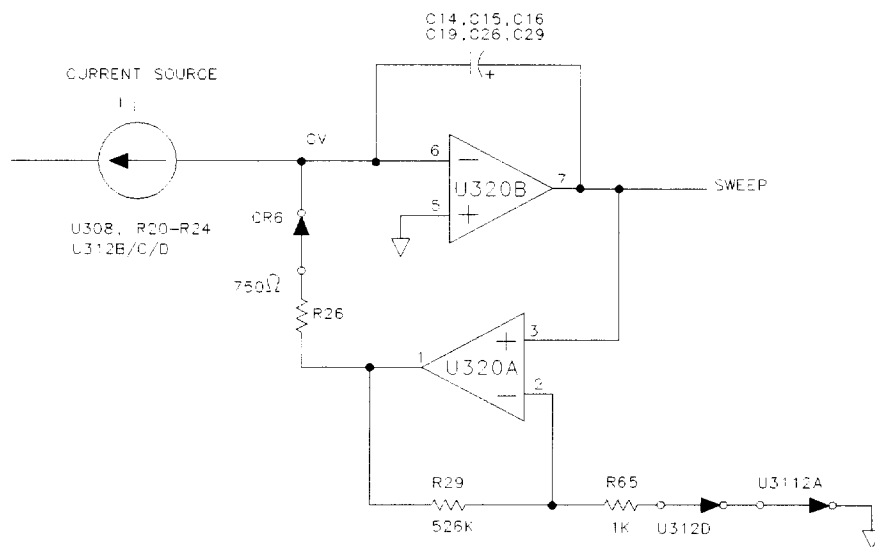
The integration is initiated by HSCAN going high. This opens U312A which places the output of U320A near −15 Vdc, turning CR6 off and allowing the output of integrator U320B to ramp from 0 V to +10 Vdc. The analyzer's ADC (via the scan ramp attenuator U320B pin 7) monitors the scan ramp at U325A pin 1. When the ramp reaches +10 V (for single-band sweeps), HSCAN is brought low and the integration ends. During normal non-fast-zero spans (sweep times >30 ms), comparators U319A and B are high. This turns off diodes CR1, CR2 and turns on transistors Q1 and Q2. The integrating current has a maximum value of 236  $\mu$ A.

During retrace, HSCAN is low, closing U306B and U312A. See Figure 10-10. The output of U320A tries to go high, turning CR6 on and sourcing current through R26. This current discharges the capacitors in the integrator, forcing U320B pin 7 toward 0 Vdc. Ultimately, the output of U320B will be brought and held to 0 V by U320A supplying a current equal to that which is sunk by the current source. For more information, refer to “First-LO Span Problems (Multiband Sweeps)” in this chapter.



sp132e

**Figure 10-9. Simplified Sweep Generator**



sp133e

**Figure 10-10. Simplified Sweep Generator during Retrace**

---

## Sweep Generator Circuit

### (for Spectrum Analyzers with 2000 s max. Sweep Time)

The sweep generator circuitry generates a ramp from 0 to 10 volts during the sweep time. The available sweep times range from 50  $\mu$ s to 2,000 seconds. The sweep times are generated in two different ranges, a 50  $\mu$ s to 30 ms range and a 50 ms to 2,000 second range. The 50  $\mu$ s to 30 ms range is only needed for analog zero span sweeps.

The sweep generator is controlled with an 8-bit latch and the control signal HSCAN. The latch, U308, controls the sweep rate. HSCAN determines when to reset the scan ramp and when to let it sweep.

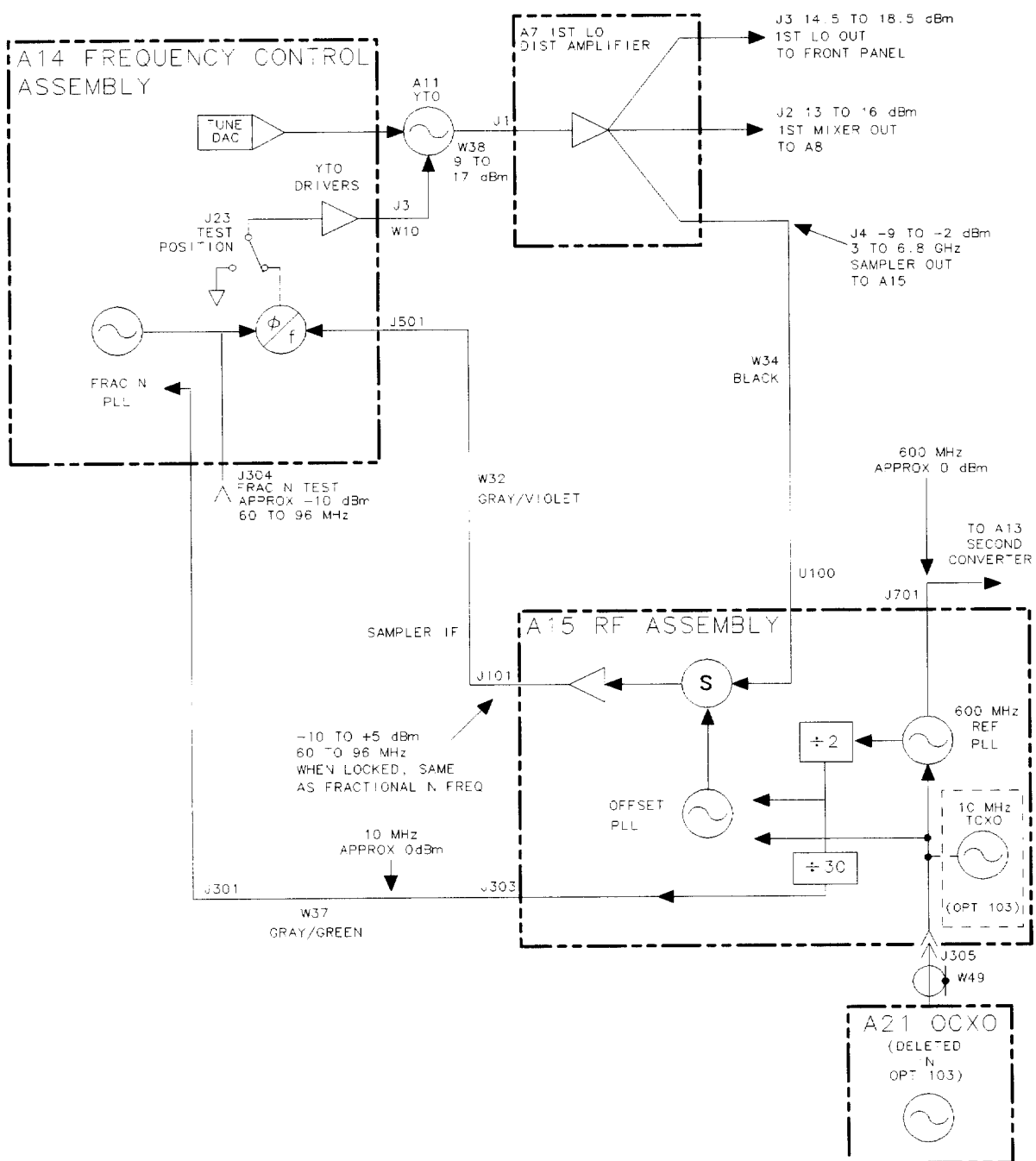
Operation of the 50 ms to 2,000 second range will be described using a 50 ms sweep time as the example. For a 50 ms sweep time, Q1 shorts out C16. The D to A converter U307, has zero output current. U334A is a buffer with zero offset, because there is no current coming out of U307. The buffering of U334 makes the base-emitter voltages on Q3A and Q3B the same. These two transistors are matched, so their collector currents should be identical when their base-emitter voltages are identical. The emitter current of Q3B is 200  $\mu$ A, therefore the emitter current of Q3A is 200  $\mu$ A and the sweep ramp is generated by C14. The sweep time is given by the formula:

$$sweeptime = capacitance(C14) \frac{\Delta V}{current}$$

The DAC setting is increased for longer sweep times. This increases the current sunk by the DAC output U307 pin 4, which increases the emitter voltage on Q3A, decreasing the base-emitter voltage drop. Q3A acts as an exponentiator and reduces its collector current, creating a slower sweep ramp.

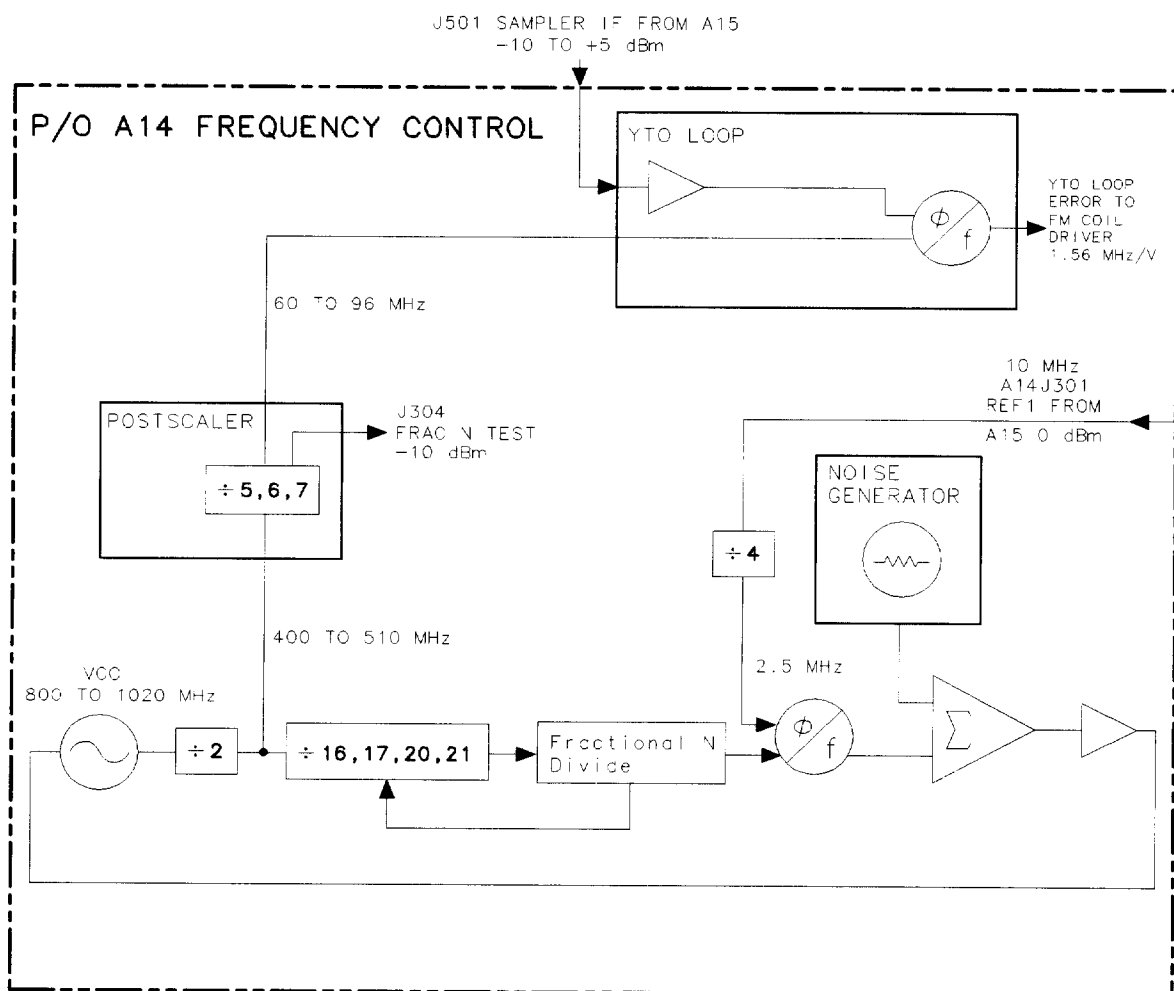
For the shorter sweep times, 50  $\mu$ s to 30 ms, Q1 is opened putting C16 in series with C14. This changes the effective capacitance from 1  $\mu$ F to 1,000 pF, or a reduction of 1,000 to 1.

The HSCAN signal uses Q2 to reset the ramp. Q2 shorts the integrator and sets its output nominally to ground.



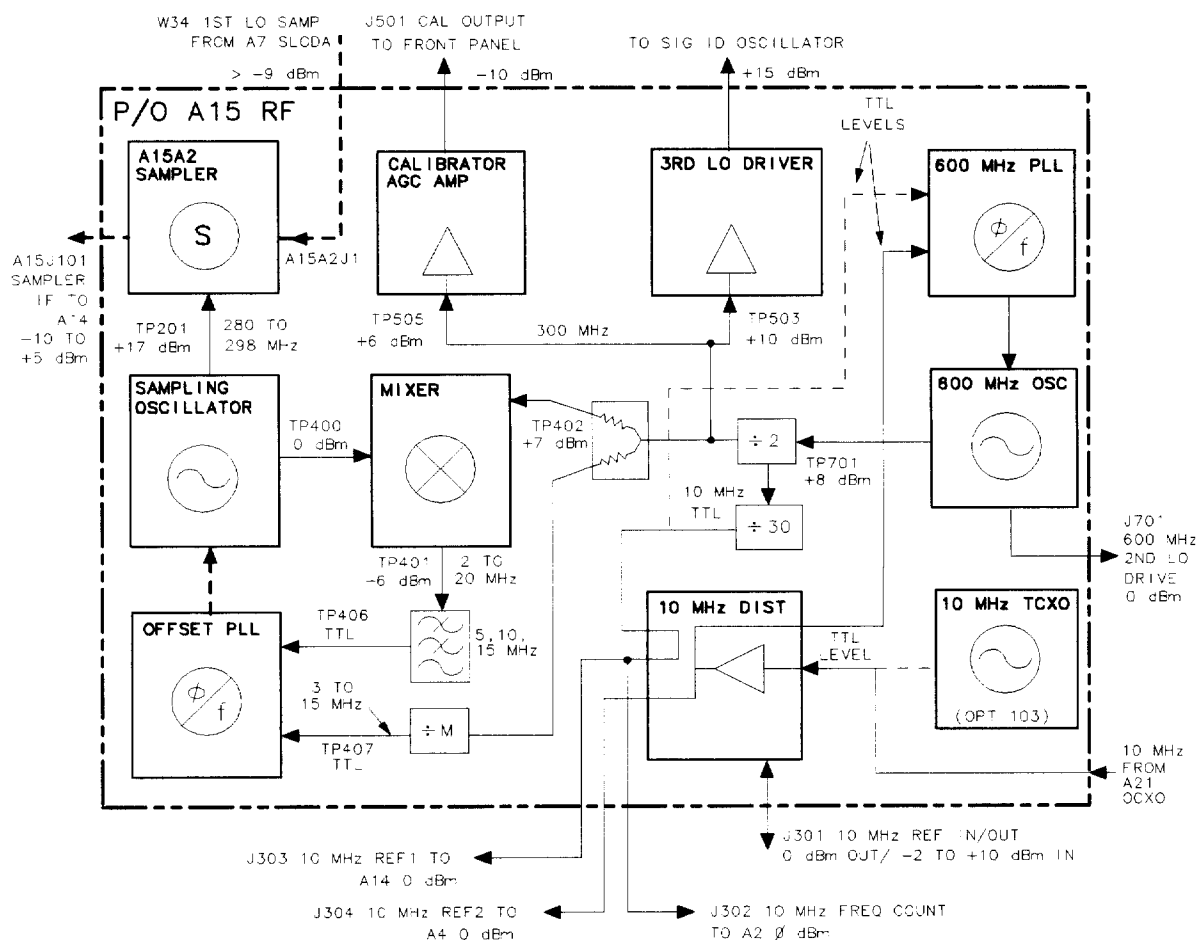
sj147e

Figure 10-11. Simplified Synthesizer Section



sj146e

**Figure 10-12. Simplified A14 Assembly Block Diagram**



sp134e

**Figure 10-13. Simplified A15 Assembly Block Diagram**

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## A21 OCXO

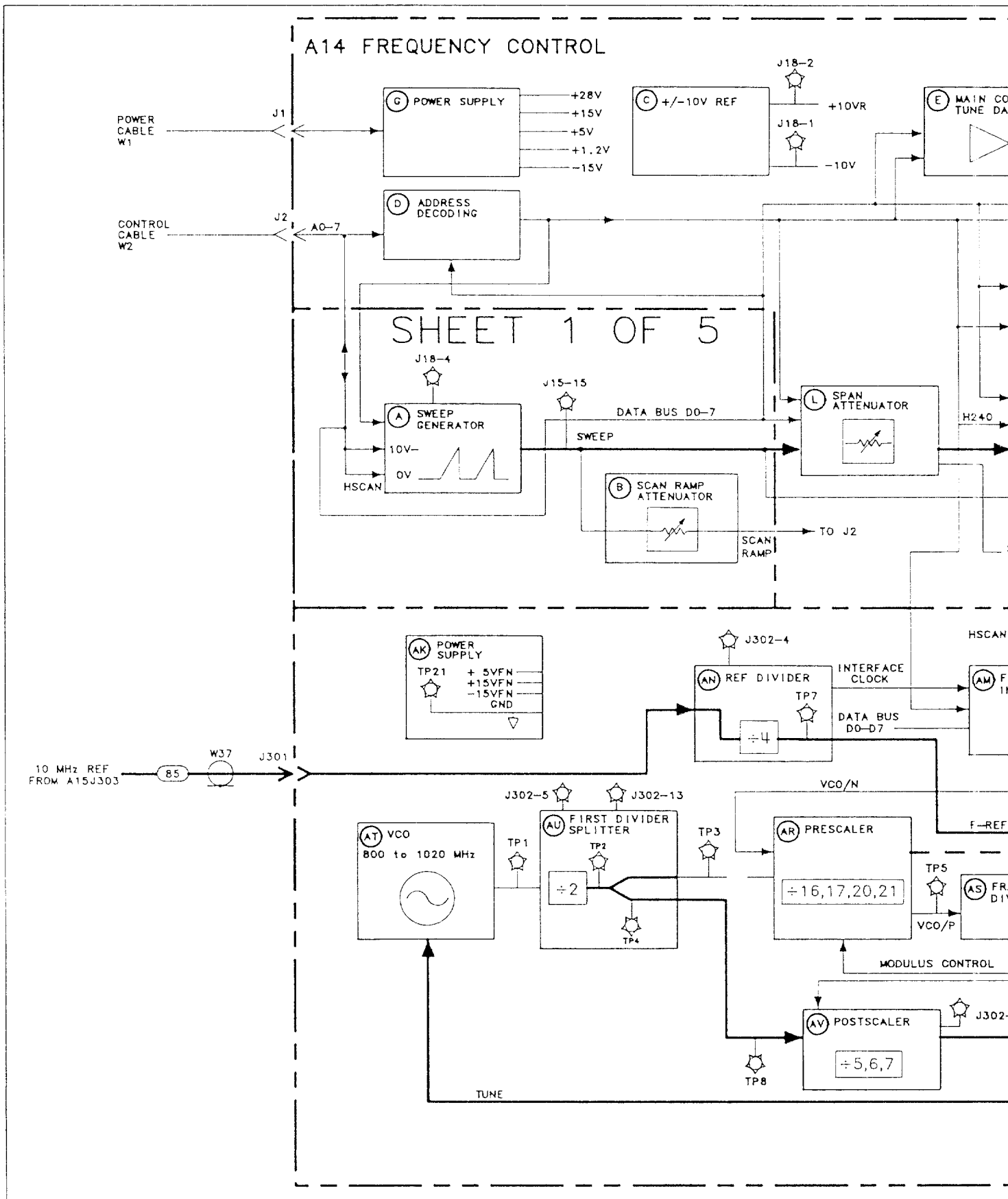
The spectrum analyzer uses an oven-controlled crystal oscillator (OCXO). It is deleted in Option 103 and replaced by a temperature-compensated crystal oscillator (TCXO), located on the A15 RF assembly. Connectors J305 and J306 on the A15 RF assembly are located where the TCXO would be installed in an Option 103. The oven in the OCXO is powered only when the spectrum analyzer is powered on; there is no standby mode of operation. The OCXO's oscillator operates only when the internal frequency reference is selected. Control line HEXT (High = EXternal frequency reference) is inverted by A15U303B (Refer to the A15 RF assembly schematic diagram, block M, sheet 2 of 4) to generate LEXT. LEXT is sent to the OCXO via A15J306 pin 4. When LEXT is low, the oscillator in the OCXO will be turned off.

Replacement OCXOs are factory adjusted after a complete warmup and after the specified aging rate has been achieved. Thus, readjustment should typically not be necessary after OCXO replacement, and is generally not recommended.

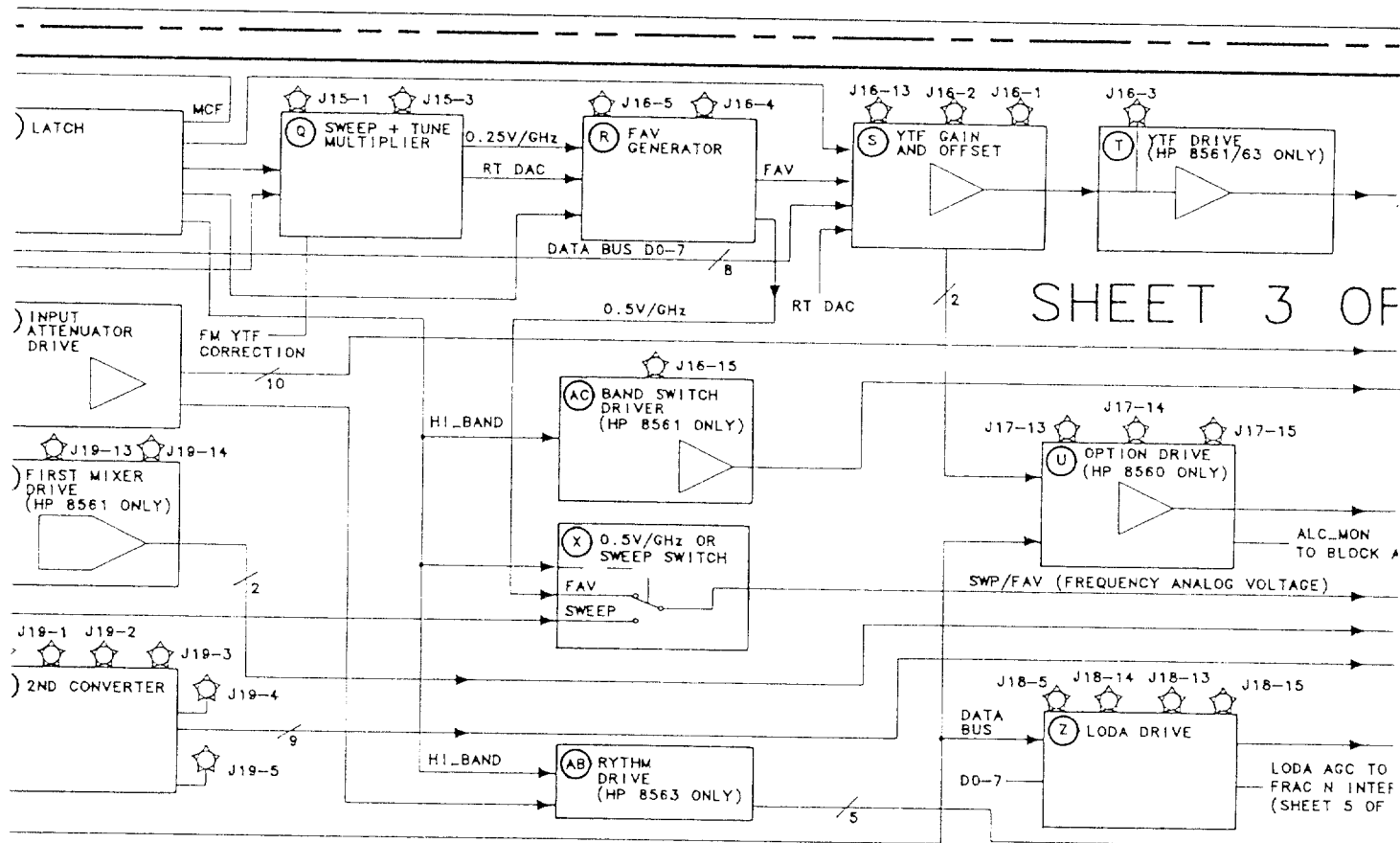
If adjustment is necessary, the spectrum analyzer must be on continuously for a minimum of 24 hours immediately prior to oscillator adjustment to allow both the temperature and frequency of the oscillator to stabilize. Failure to allow sufficient stabilization time could result in oscillator misadjustment.

Check operation of the A21 OCXO as follows:

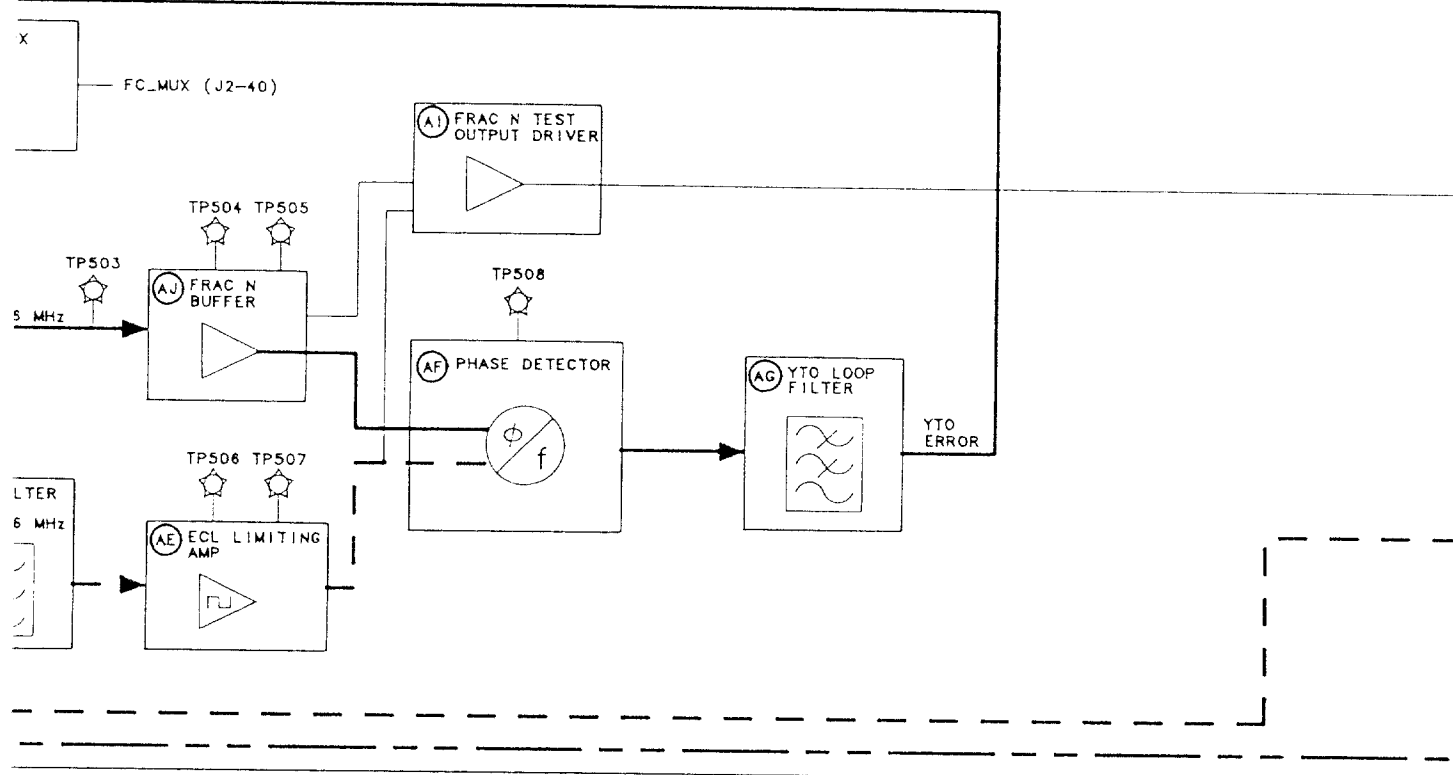
1. Disconnect W49 (Coax 82) from A15J305. Connect the output of W49 to the input of another spectrum analyzer.
2. Check that the fundamental frequency is 10 MHz and that the power level is 0 dBm  $\pm$ 3 dB. Also check that the harmonics are at least -25 dBc. Excessive harmonics can generate spurious responses on the fractional N oscillator on the A14 frequency control assembly.
3. If the OCXO has no output, check A15J306 pin 1 for +15 Vdc. Check A15J306 pin 4 for a TTL-high level.
4. If A15J306 pin 4 is at a TTL-low level, press **AUX CTRL** and **REAR PANEL**. Press **10 MHz EXT INT** until INT is underlined. A15J306 pin 4 should read a TTL-high level. Press **10 MHz EXT INT** until EXT is underlined. A15J306 pin 4 should read a TTL-low level.

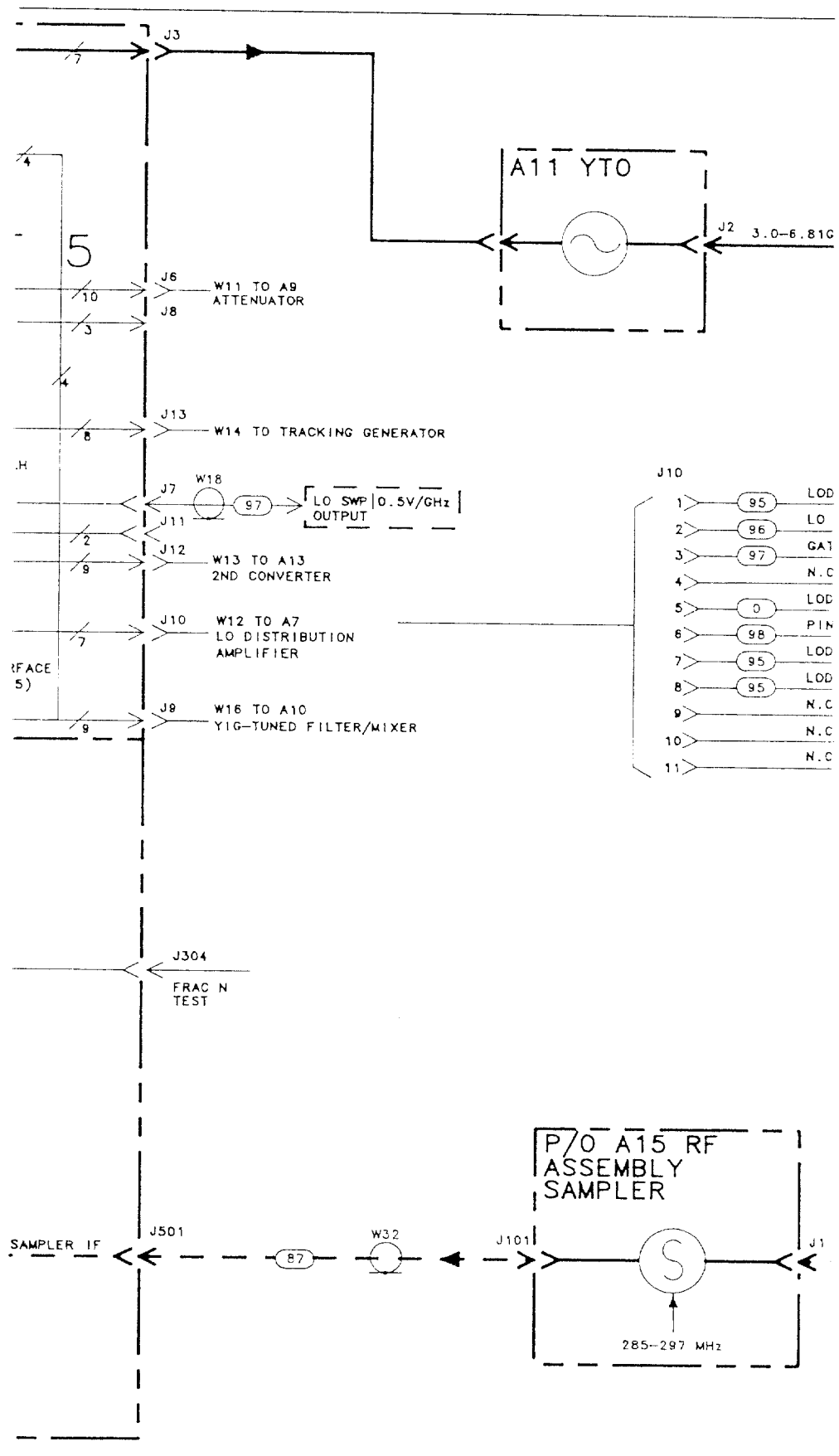






OF 5





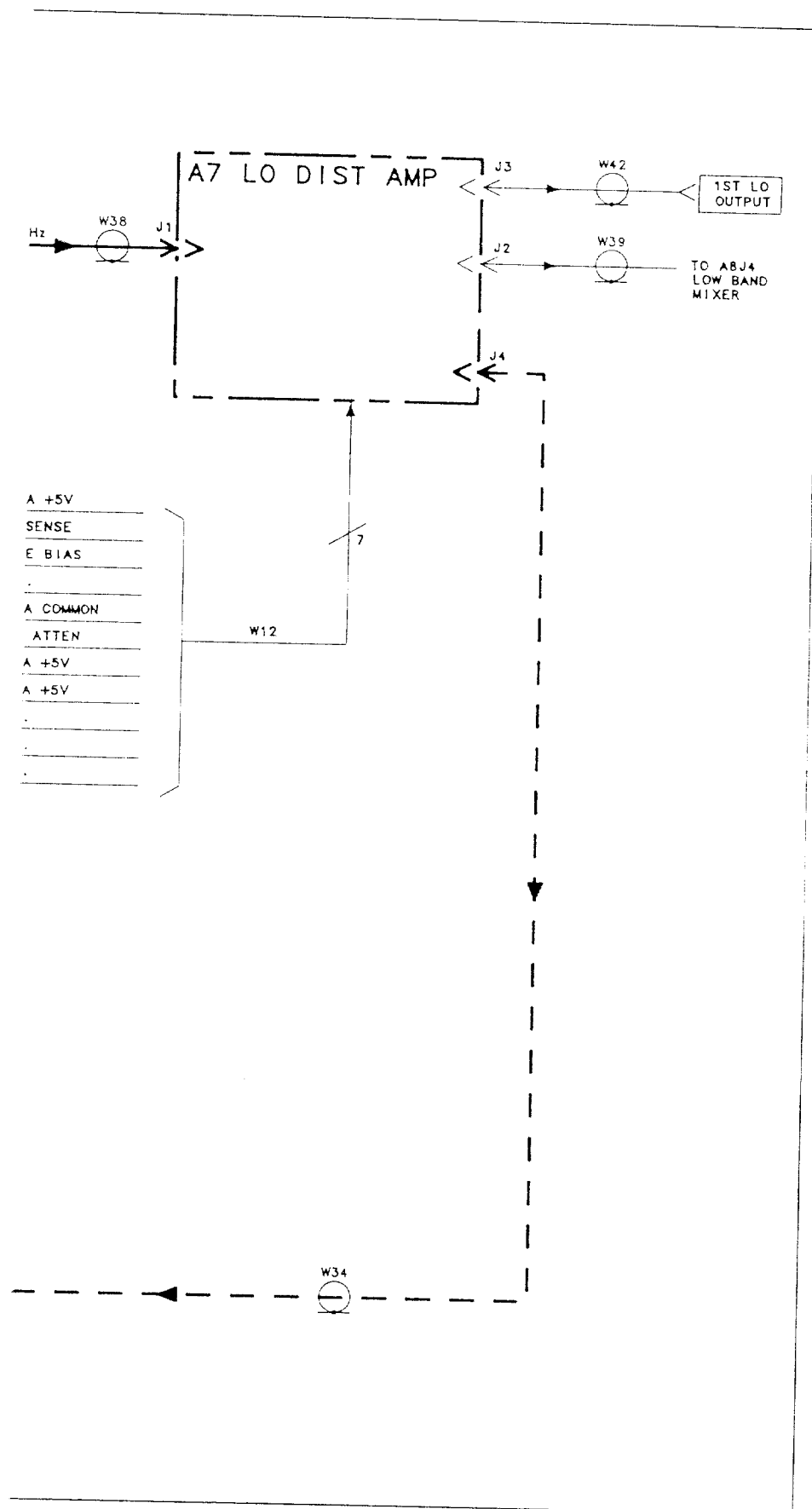
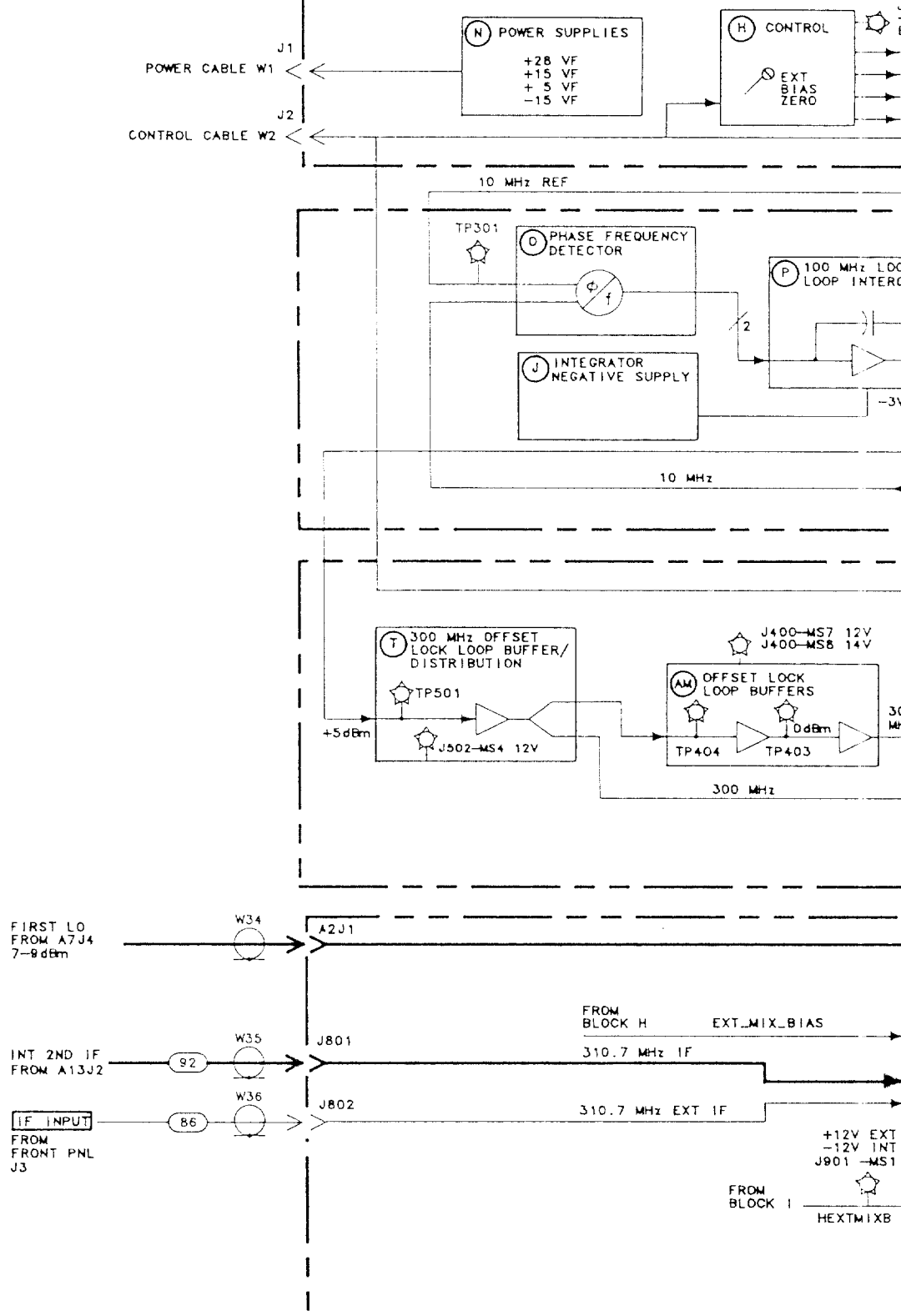
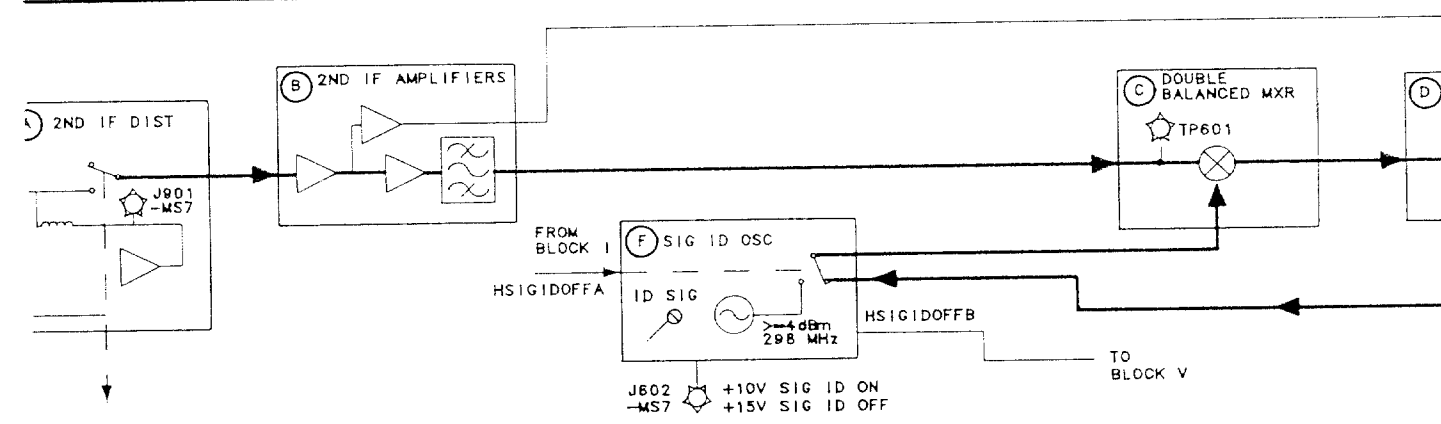
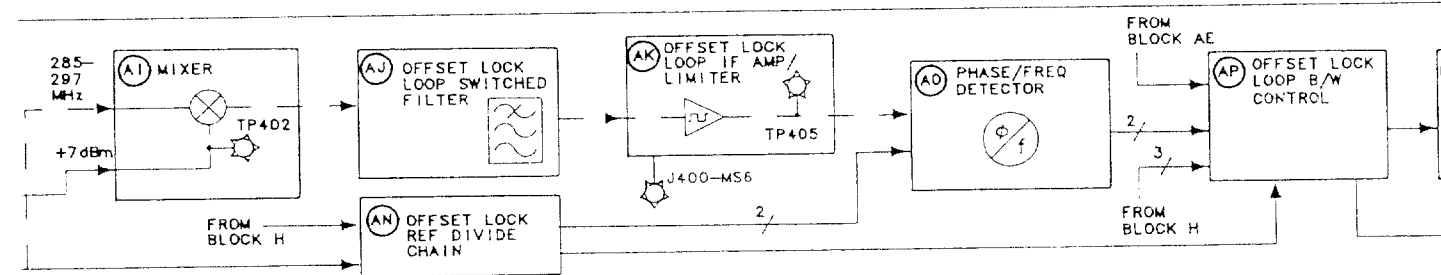
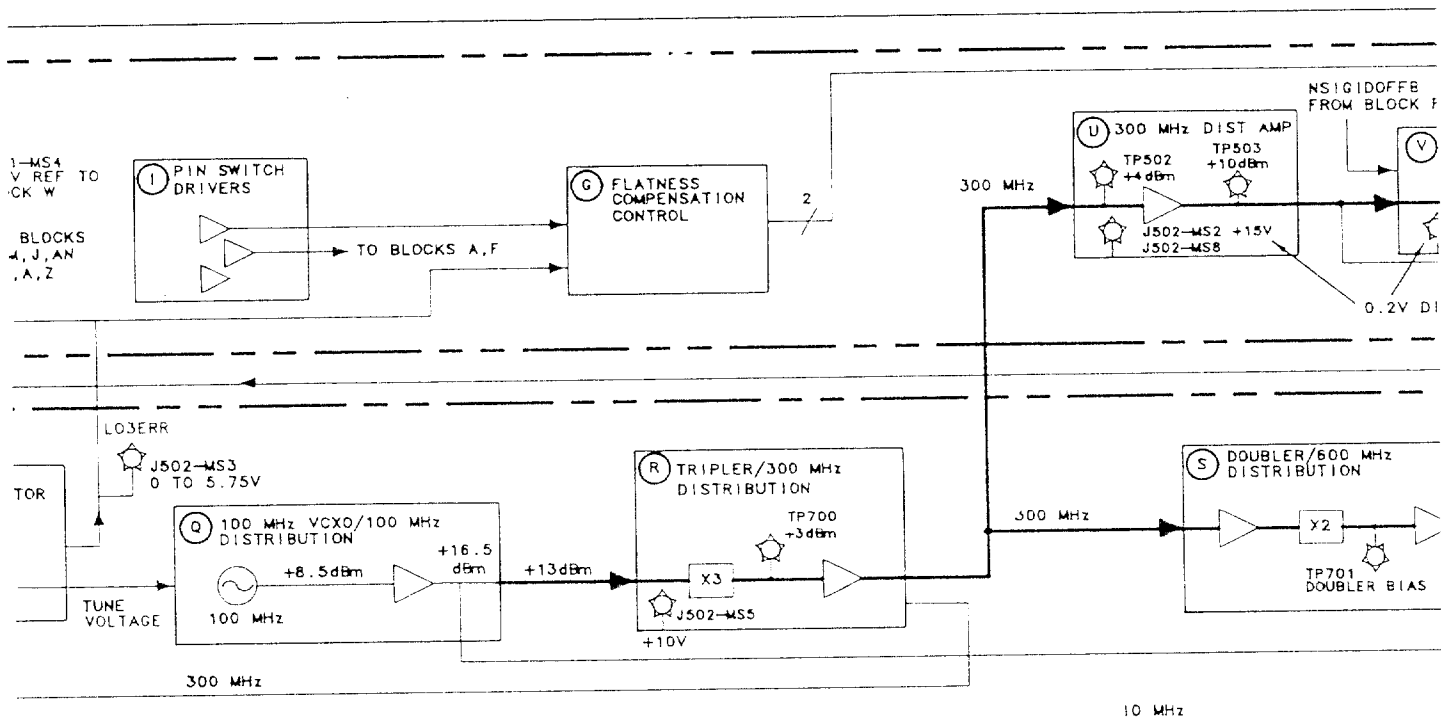
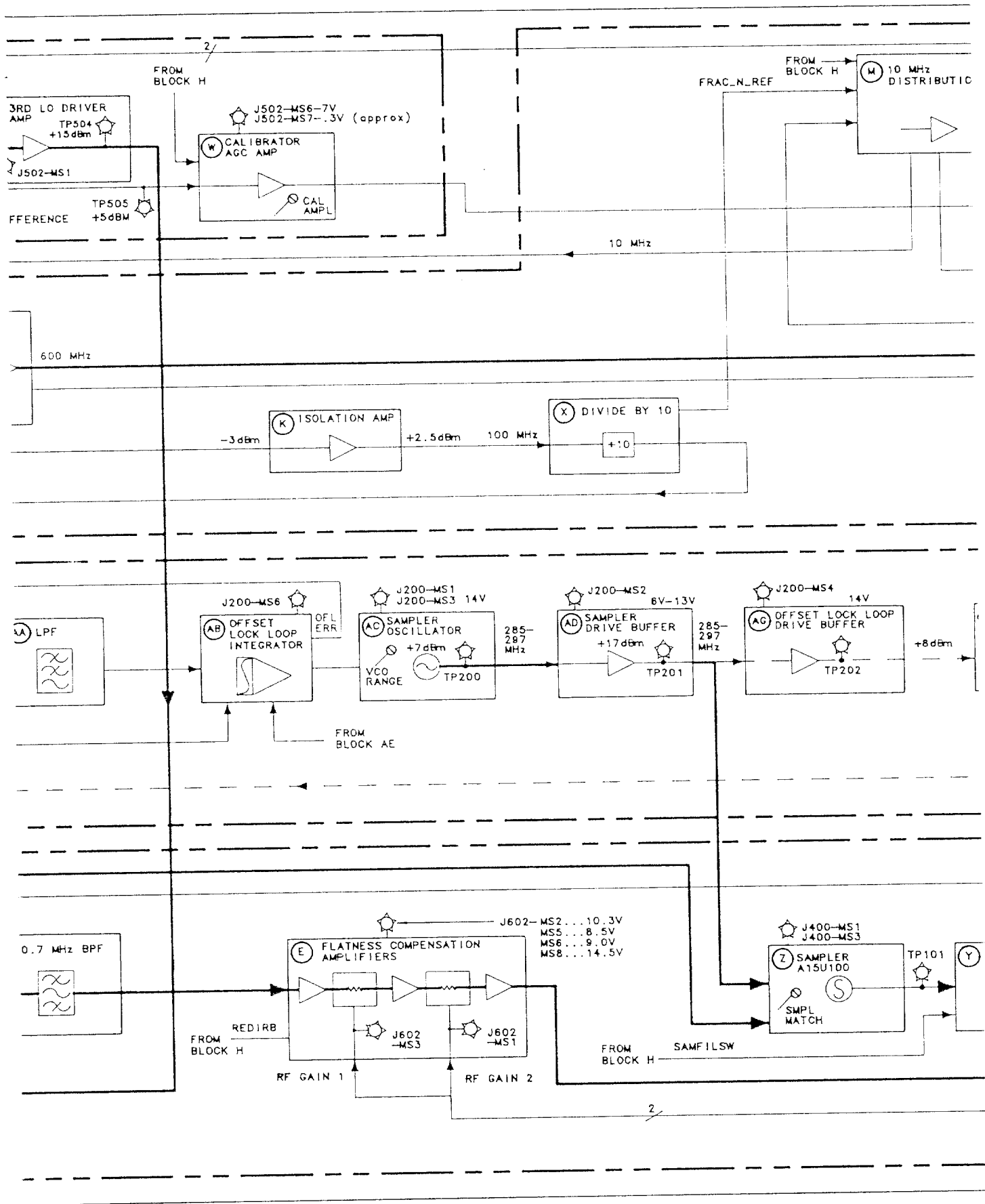


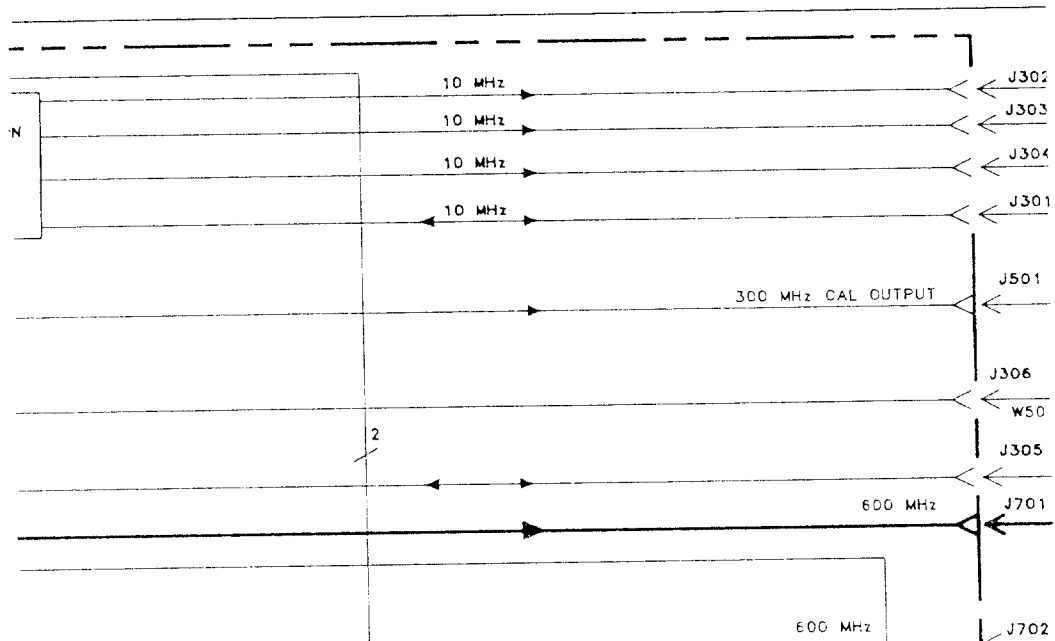
FIGURE 10-14 FREQUENCY CONTROL BLOCK DIAGRAM

A15 RF  
SHEET 1 OF 4

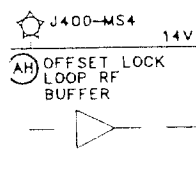




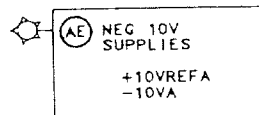




SHEET 2 OF 4

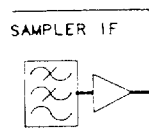


J200-MSB



TO BLOCKS  
AB AND AP

SHEET 3 OF 4



TO BLOCK H  
U903, PIN 12

310.7 MHz J803

J101

10.7 MHz J601

SHEET 4 OF 4

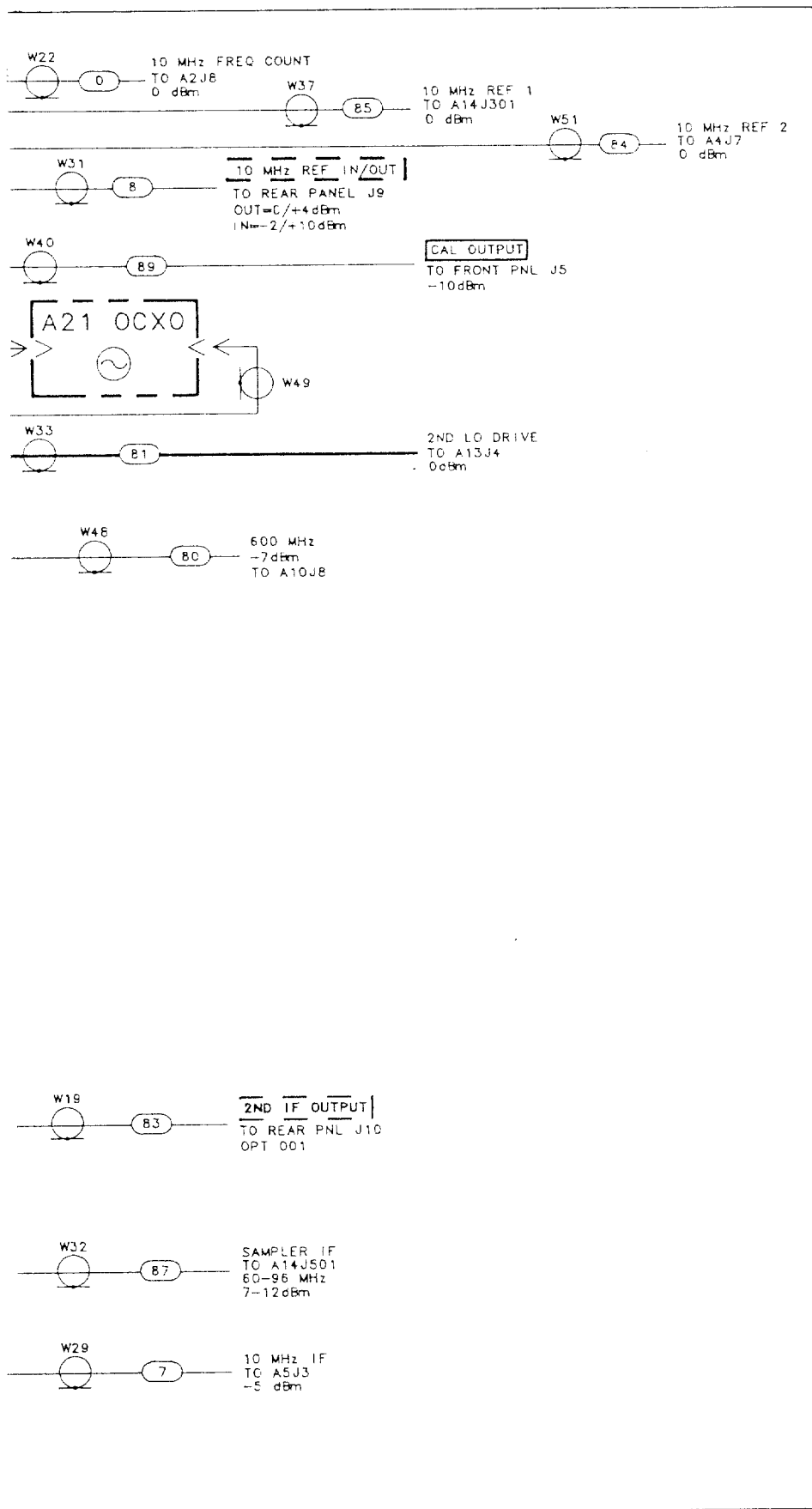
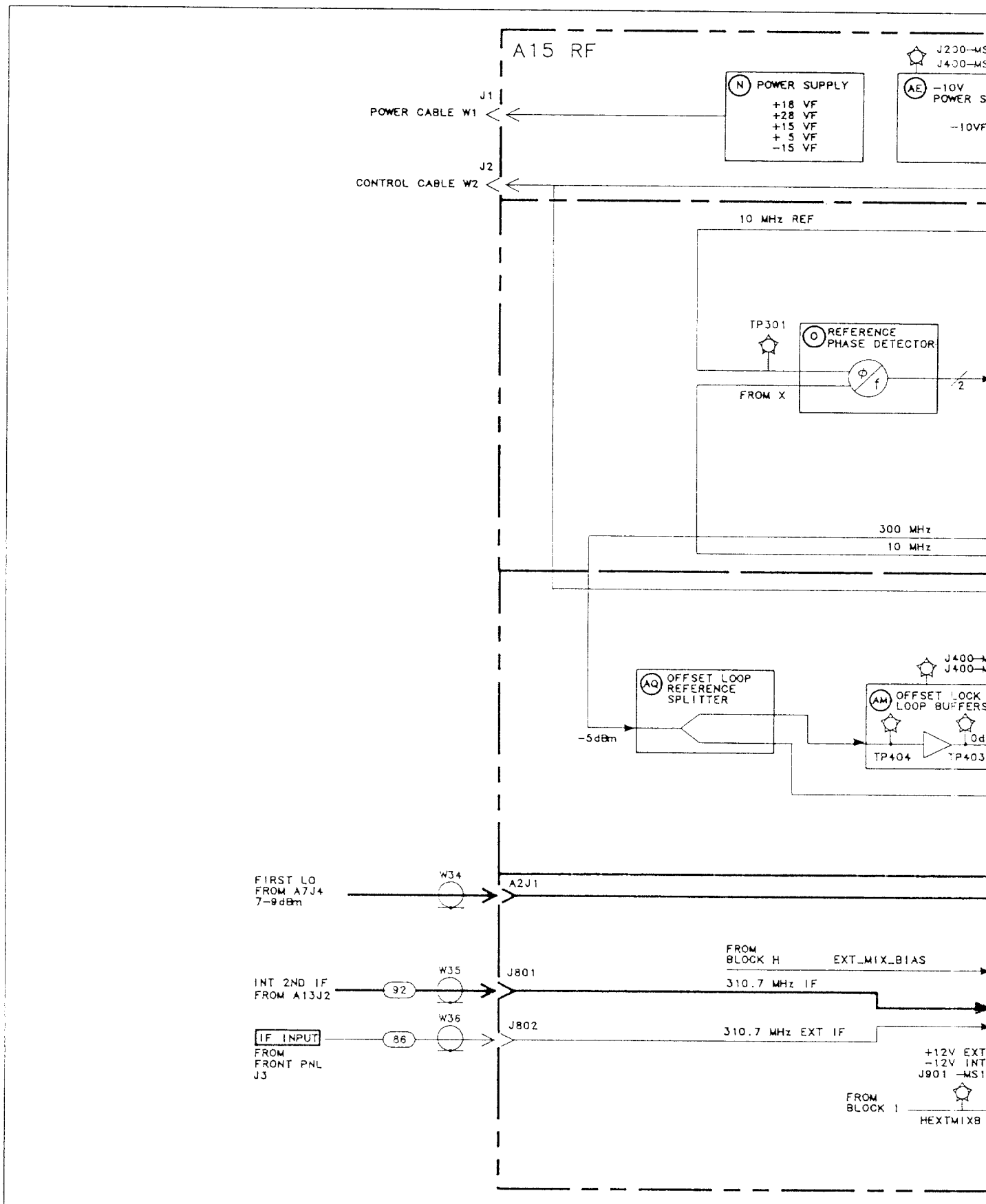
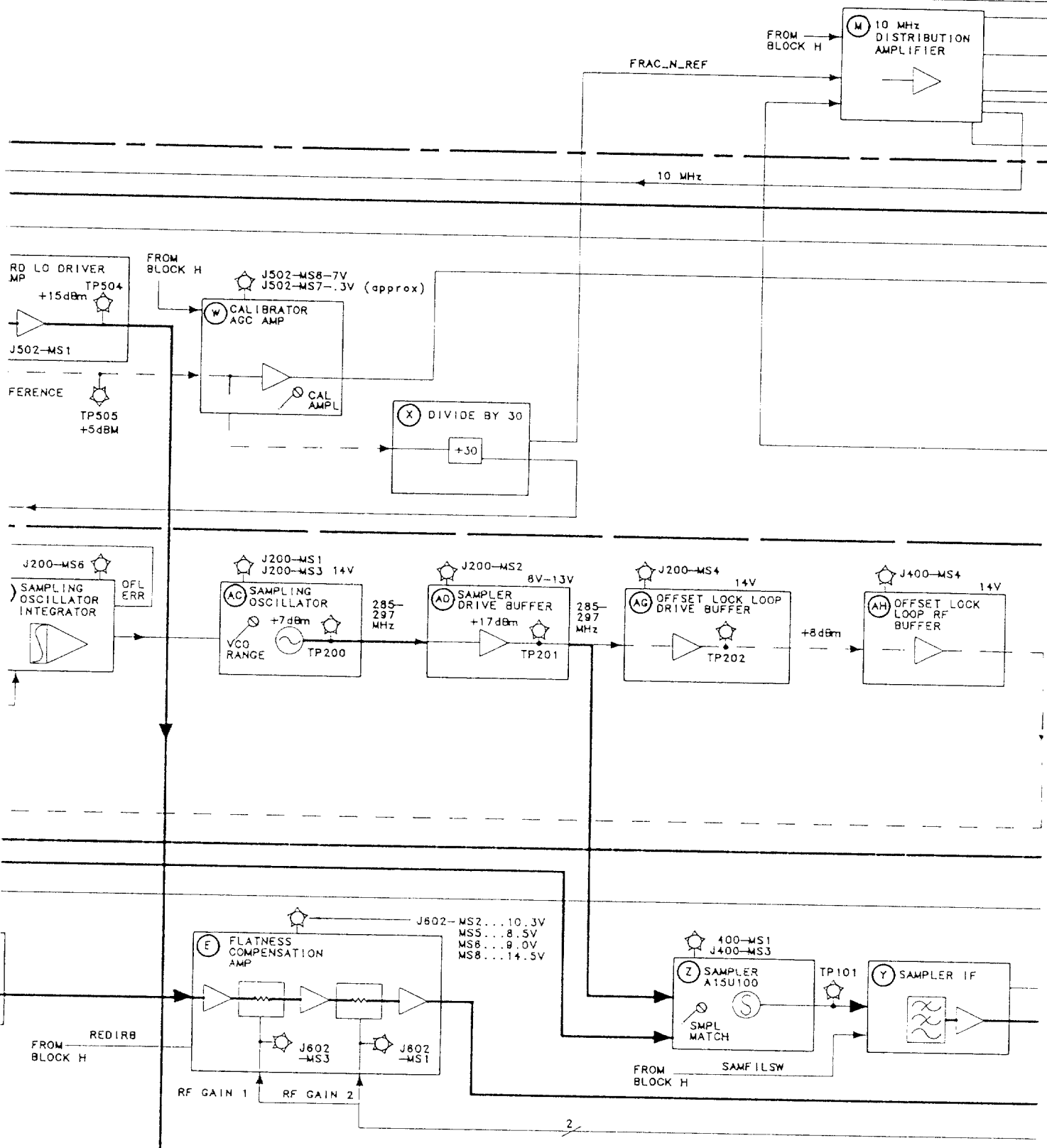
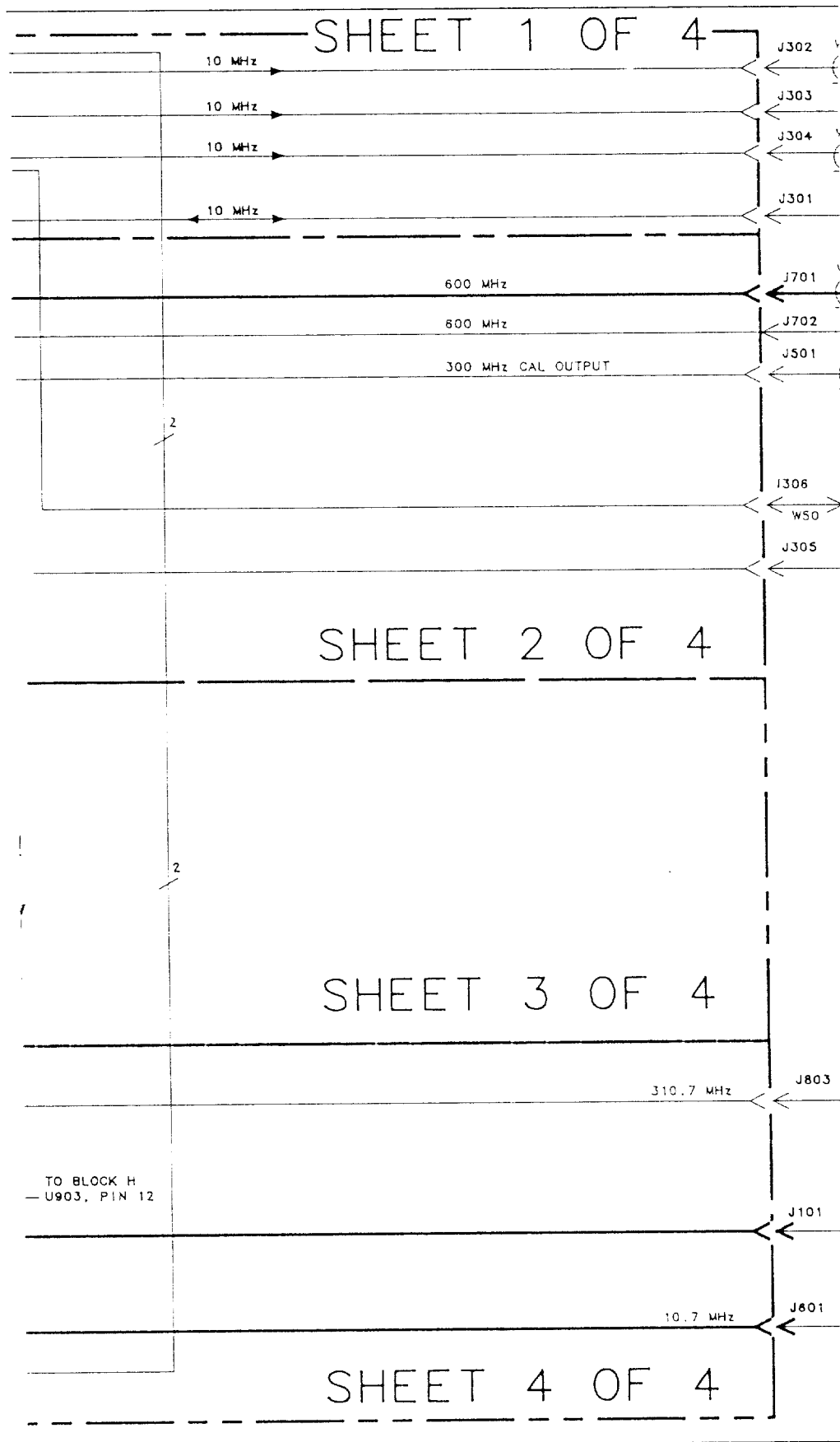


FIGURE 10-15. RF ASSEMBLY BLOCK DIAGRAM  
(FOR A15 08563-60054, 08563-60055, OR 08563-60056).









# SYNTHESIZER SECTION

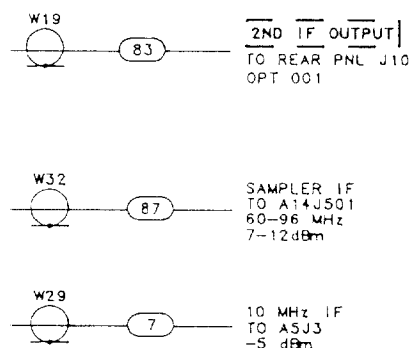
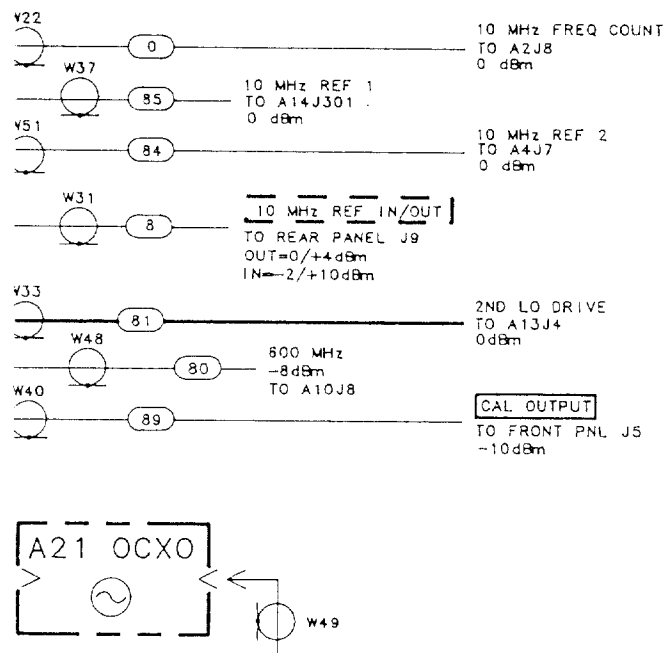


FIGURE 10-16. RF ASSEMBLY BLOCK DIAGRAM  
EARLIER THAN 08563-60054, 08563-60055, OR 08563-60056.

## RF Section

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The RF section converts the input signal to a 10.7 MHz IF (Intermediate Frequency). See Figure 11-5 for a detailed block diagram.

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**Note**           The block diagrams for the A14 and A15 assemblies are located in Chapter 10, “Synthesizer Section.”

---

Troubleshooting Using the TAM  
 Low Band Problems (50 Hz to 2.9 GHz)  
 Low Band Problems  
 A7 LODA (LO Distribution Amplifier)  
 A8 Low Band Mixer  
 A9 Input Attenuator  
 A13 Second Converter  
 A14 Frequency Control Assembly  
     A7 LODA Drive  
 A15 RF Assembly  
     Confirming a Faulty Third Converter  
     Confirming a Third Converter Output  
     Third Converter  
     Flatness Compensation Control  
     Control Latches  
     SIG ID Oscillator (Option 008)  
     10 MHz Reference  
 A10 Tracking Generator (Option 002)  
     Block Diagram Description  
     Output Goes Unleveled (ERR 900 or ERR 901)  
     Excessive Residual FM  
     Flatness Out-of-Tolerance  
     Vernier Accuracy Out-of-Tolerance  
     Harmonic/Spurious Outputs Too High  
     Power Sweep Not Functioning Properly  
     No Power Output

---

**Caution**       All of the RF assemblies are extremely sensitive to Electrostatic Discharge (ESD). For further information regarding electrostatic cautions, refer to “Electrostatic Discharge” in Chapter 1.

---

**Table 11-1. Automatic Fault Isolation References**

| <b>Suspected Circuit Indicated<br/>by Automatic Fault Isolation</b> | <b>Manual Procedure to Perform</b>                           |
|---------------------------------------------------------------------|--------------------------------------------------------------|
| Check 2nd IF Amplifier                                              | Third Converter                                              |
| Check 2nd IF Distribution                                           | Third Converter                                              |
| Check 10.7 MHz IF Out of Double Balanced Mixer                      | Third Converter                                              |
| Check 300 MHz CAL OUTPUT                                            | Calibrator Amplitude Adjustment in Chapter 2                 |
| Check A7 1st LO Distribution Amplifier                              | A7 LODA (LO Distribution Amplifier)                          |
| Check A8 Low Band Mixer                                             | A8 Low Band Mixer                                            |
| Check A9 Input Attenuator                                           | A9 Input Attenuator                                          |
| Check A13 Second Converter                                          | A13 Second Converter                                         |
| Check A13J2 INT 2nd IF                                              | A13 Second Converter ( <i>steps 1 to 6</i> )                 |
| Check A15 Control Latches                                           | Control Latches                                              |
| Check A15J601 10.7 MHz                                              | Third Converter Output                                       |
| Check External 10 MHz Reference Operation                           | 10 MHz Reference ( <i>steps 5 to 11</i> )                    |
| Check Gain of Flatness Compensation Amplifier                       | Third Converter                                              |
| Check INT 10 MHz Reference Operation                                | 10 MHz Reference ( <i>steps 1 to 4</i> )                     |
| Check LO Feedthrough                                                | Low Band Problems (1 kHz to 2.9 GHz) ( <i>steps 1 to 3</i> ) |
| Check LO Power                                                      | Low Band Problems ( <i>steps 4 to 9</i> )                    |
| Check PIN Switch                                                    | PIN Switch                                                   |
| Check PIN Switches in SIG ID Oscillator                             | SIG ID Oscillator                                            |
| Check Second Converter Control                                      | A13 Second Converter                                         |
| Check SIG ID Oscillator                                             | Signal ID Oscillator Adjustment in Chapter 2                 |
| Check SIG ID Oscillator Operation                                   | SIG ID Oscillator                                            |
| Check Third Converter                                               | Low Band Problems ( <i>step 10</i> )                         |

---

## Low Band Problems (50 Hz to 2.9 GHz)

1. Disconnect all inputs from the front-panel INPUT 50 $\Omega$  connector.
2. Set the HP 8560E to the following settings:

|                   |             |
|-------------------|-------------|
| Center frequency  | ..... 0 Hz  |
| Span              | ..... 1 MHz |
| Input attenuation | ..... 0 dB  |
3. The LO feedthrough's amplitude observed on the display should be between  $-6$  and  $-30$  dBm.

---

|             |                                                                                                                                                                                                                  |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note</b> | The marker will not peak search on the LO feedthrough when in a non-zero span. To measure the LO feedthrough amplitude with the markers, set the span to 0 Hz and center frequency to 0 Hz. Press <b>MKR</b> ON. |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

---

4. If the LO feedthrough's amplitude is within limits, but signals are low, the RF path following the A8 Low Band Mixer is operating properly.
5. If the LO feedthrough's amplitude is higher than  $-5$  dBm (signal will be "clipped" at top of screen) and signals are low in amplitude, suspect a defective A8 Low Band Mixer.
6. Check A13 Second Converter mixer diode bias at A14J19 pin 1. The bias voltage should be between  $-150$  and  $-900$  mVdc.
7. Troubleshoot the signal path. Refer to the power levels listed on Figure 11-3, RF Section Troubleshooting Block Diagram.

---

## Low Band Problems

1. On the HP 8560E press **PRESET** and **REALIGN LO & IF**. If any error messages are displayed, refer to "Error Messages" in Chapter 6.
2. Perform "External Mixer Amplitude Adjustment" in Chapter 2. If this adjustment cannot be completed, perform the steps located in "Third Converter" in this chapter.
3. Perform the "First LO Output Amplitude" performance test (Refer to the *HP 8560 E-Series Spectrum Analyzer Calibration Guide* or use the TAM functional test).
4. If the performance test fails, perform the "First LO Distribution Amplifier Adjustment" in Chapter 2. If the adjustment fails, set the HP 8560E to the following settings:

|                  |               |
|------------------|---------------|
| Center frequency | ..... 300 MHz |
| Span             | ..... 0 Hz    |
5. Place the jumper on A14J23 in the TEST position. Remove W38 from the input of the A7 LODA.
6. Use a power meter or another spectrum analyzer to measure the output of A11 YTO. The power should be between  $+2$  dBm and  $+13$  dBm.
7. Reconnect W38 to the LODA. Place the jumper on A14J23 in the NORM position.

11. If this voltage is not within the correct range, refer to “LO Distribution Amplifier Adjustment” in Chapter 2, “Adjustment Procedures.”
12. If the voltage varies between 0 Vdc and –2 Vdc, adjust the GATE BIAS for a DVM reading within  $\pm 10$  mV of the GATE BIAS voltage listed on A7 LODA’s label. If the voltage does not vary between 0 Vdc and –2 Vdc, troubleshoot the A14 frequency control assembly.
13. Disconnect the jumper from A14J19 to A14J10. Press **LINE** to turn spectrum analyzer off. Reconnect W12 to A14J10. Press **LINE** to turn spectrum analyzer on.
14. If the DVM reading changes significantly, the A7 LODA is probably defective.

---

## A8 Low Band Mixer

1. Connect the HP 8560E CAL OUTPUT to INPUT 50 $\Omega$ .
2. Set the HP 8560E as follows:  
Center frequency ..... 300 MHz  
Span ..... 0 Hz  
Input attenuation ..... 10 dB
3. Using another spectrum analyzer, check for approximately –21 dBm (300 MHz) at the input of A8. (This level can easily be measured at the output of FL1 by disconnecting W45 from FL1.)
4. If the level at the input of A8 is less than –25 dBm, suspect FL1 low-pass filter, or A9 input attenuator. Refer to power levels shown on Figure 11-5, RF Section Troubleshooting Block Diagram.
5. Check for approximately –30 dBm (3.9107 GHz) at the output of A8. (This level can easily be measured at the output of FL2 by disconnecting W57 from FL2.)
6. If the level at the output of A8 is less than –35 dBm, suspect A8 low band mixer or FL2 low-pass filter.

## A13 Second Converter

**Caution** The A13 assembly is extremely sensitive to Electrostatic Discharge (ESD). For further information regarding electrostatic cautions, refer to “Electrostatic Discharge Information” in Chapter 1.

1. Connect the HP 8560E CAL OUTPUT to the INPUT 50 $\Omega$  connector.
2. Set the HP 8560E to the following settings:

|                   |              |
|-------------------|--------------|
| Center frequency  | .....300 MHz |
| Span              | ..... 0 Hz   |
| Input attenuation | ..... 10 dB  |
3. Disconnect W35 (coax 92) from A13J2.
4. Connect a test cable from A13J2 to the input of another spectrum analyzer.
5. Tune the other spectrum analyzer to 310.7 MHz. The signal displayed on the other spectrum analyzer should be approximately  $-38$  dBm.
6. Remove the test cable from A13J2 and reconnect W35 to A13J2.
7. Disconnect W33 (coax81) from A13J4 and connect W33 through a test cable to the input of another spectrum analyzer.
8. Tune the other spectrum analyzer to a center frequency of 600 MHz.
9. If a 600 MHz signal is not present, or its amplitude is less than  $-5$  dBm, the fault is probably on the A15 RF assembly.
10. Reconnect W33 to A13J4.
11. Connect a DVM's positive lead to A14J19 pin 15 and the negative lead to A14J19 pin 6.
12. If the DVM does not measure between  $+14.0$  Vdc and  $+15.0$  Vdc perform the following:
  - a. Press **LINE** to turn spectrum analyzer off and disconnect W13 from A14J12.
  - b. Press **LINE** to turn spectrum analyzer on and set the spectrum analyzer to the following settings:

|                  |              |
|------------------|--------------|
| Center frequency | .....300 MHz |
| Span             | .....10 MHz  |
  - c. The voltage should measure  $+15$  Vdc  $\pm 0.2$  V. If the voltage measures outside this limit, the A14 frequency control assembly is probably defective.
  - d. Press **LINE** to turn spectrum analyzer off, reconnect W13 to A14J12, and press **LINE** to turn spectrum analyzer on. Set the HP 8560E to the following settings:

|                  |              |
|------------------|--------------|
| Center frequency | .....300 MHz |
| Span             | ..... 0 Hz   |
13. Move the DVM's positive lead to A14J19 pin 1. The voltage should measure between  $-150$  mVdc and  $-800$  mVdc. If the voltage measures outside this limit, the A13 Second Converter is probably defective.

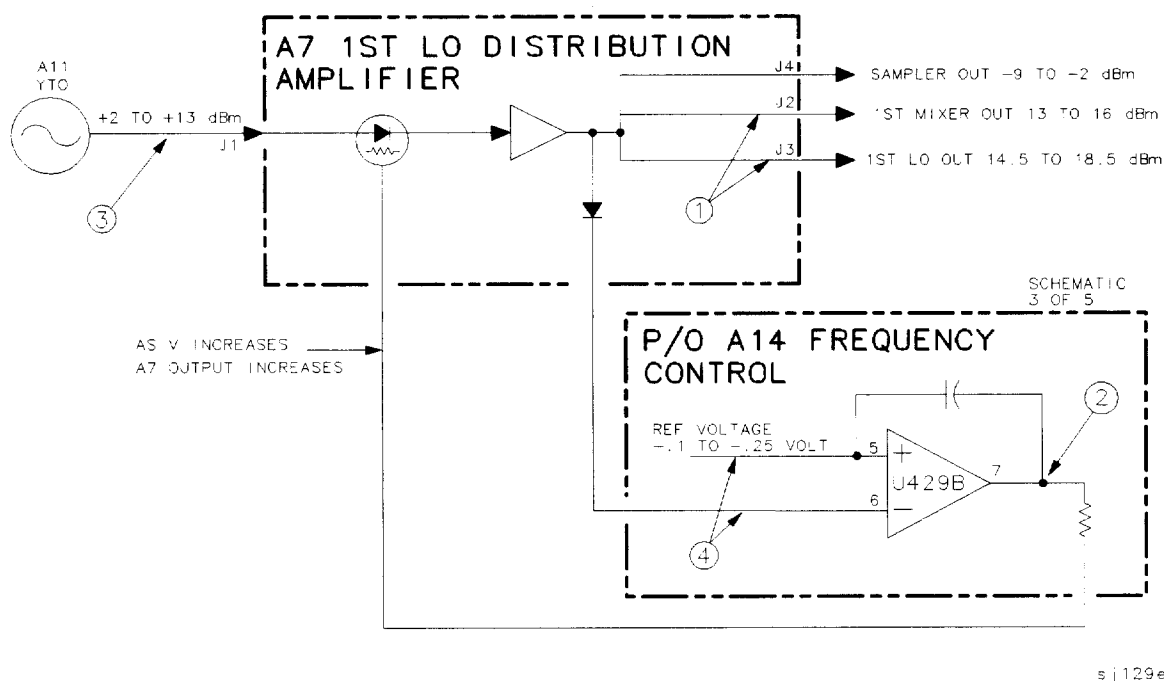


Figure 11-2. A7 LODA Drive

## A15 RF Assembly

**Note** The block diagrams for the A14 and A15 assemblies are located in Chapter 10, "Synthesizer Section."

### Confirming a Faulty Third Converter

1. Perform the "IF Input Amplitude Accuracy" performance test in the *HP 8560 E-Series Spectrum Analyzer Calibration Guide* if Opt on 002 is not present. This exercises most of the third converter.
2. If the performance test fails or Option 002 is present, perform the "External Mixer Amplitude Adjustment" in Chapter 2.
3. If adjustment cannot be made, disconnect W35 (coax 92) from A15J801.
4. On the HP 8560E, press **PRESET** and set the controls to the following settings:
 

|                        |         |
|------------------------|---------|
| Center frequency ..... | 300 MHz |
| Span .....             | 0 Hz    |
5. Connect a signal generator to A15J801.

3. Disconnect W35 (coax 92) and connect a signal source to A15J801. Set the source to the following settings:

Frequency ..... 310.7 MHz  
Amplitude ..... -30 dBm

4. Use an active probe with another spectrum analyzer to measure the signal at A15TP601 (function block C). The signal should measure -17 dBm  $\pm$ 4 dB confirming the operation of the 2nd IF Amplifier.
5. Use an active probe with another spectrum analyzer to measure the 300 MHz into the third mixer's LO port. The signal should measure at least +20dBm.
6. Measure the power of the mixer's 10.7 MHz IF output. The signal level should be approximately -22 dBm.
7. Move the A2 controller assembly's WR PROT/WR ENA jumper to the WR ENA position.
8. While measuring the signal at the mixer's 10.7 MHz IF output, adjust the signal source until the level of the 10.7 MHz IF is -40 dBm.
9. On the HP 8560E, press **SGL SWP**, **CAL**, **IF ADJ OFF**, **MORE 1 OF 2**, and **FLATNESS**. Increase the gain of the flatness compensation amplifiers to maximum by entering 0 using the data keys. This sets the gains in the flatness compensation amplifiers to their maximum values.
10. Connect the other spectrum analyzer to A15J601 and measure the 10.7 MHz IF signal level. The signal should measure greater than -10 dBm. If the signal level is incorrect, continue with step 13.
11. Enter 4095 into the HP 8560E Flatness Data. The signal level at A15J601 should measure less than -36 dBm. This sets the gain of flatness compensation amplifiers to a minimum. If the signal level is incorrect, continue with step 13.
12. Check that the gain stages are properly biased and functioning.
13. Check the attenuator stages and flatness compensation control circuitry.
  - a. For minimum gain (flatness data equals 4095), RF GAIN (A15U909 pin 10) should be at -1.6 Vdc and the current through each section as measured across R667 or R668 should be about 7 mA.
  - b. For maximum gain (flatness data equals 0), RF GAIN (A15U909 pin 10) should be at approximately 0 Vdc and the current through each attenuator section should be close to 0 mA.

---

|                |                                                                                                                                         |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| <b>Caution</b> | As long as the flatness data just entered is not stored, the previously-stored flatness data will be present after the power is cycled. |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|

---

14. Move the A2 controller assembly's WR PROT/WR ENA jumper to the WR PROT position.
15. Reconnect the cable to A15J801.

1. Set the HP 8560E to the following settings:

Trigger ..... single sweep  
 SIG ID ..... on

2. Use an active probe with another spectrum analyzer to measure the signal level at A15TP602.
3. On the HP 8560E press **SGL SWP**. With each press of **SGL SWP** the spectrum analyzer alternates between the following two states:

State 1:

|                       |                                        |
|-----------------------|----------------------------------------|
| A15J901 pin 13 (LSID) | TTL low                                |
| SIG ID oscillator     | ON                                     |
| Signal at A15TP602    | 298 MHz $\pm$ 50 kHz (at least +1 dBm) |

State 2:

|                         |                                       |
|-------------------------|---------------------------------------|
| A15J901 pin 13 (LSID)   | TTL high                              |
| SIG ID oscillator       | OFF                                   |
| 3rd LO driver amplifier | Provides LO for double balanced mixer |

4. With the SIG ID oscillator on, measure the frequency at A15TP602 with a frequency counter and an active probe. If the frequency is not 298 MHz  $\pm$ 50 kHz, refer to the "SIG ID Oscillator Adjustment" procedure in Chapter 2.
5. On the HP 8560E, press **SGL SWP** until A15J901 pin 13 is at TTL low. Diodes CR603 and CR605 should be forward biased and CR604 should be reverse biased (approximately 6 Vdc reverse bias). Diodes CR501 and CR502 should be forward-biased, disabling the 3rd LO driver amplifier.
6. The voltage at the R622/R623 node should measure approximately  $-5$  Vdc, biasing Q604 on.
7. If oscillator bias voltages are correct, place a 100  $\Omega$  resistor across SAWR U602 input and output. If the SAWR has failed, this will provide the equivalent loss of a correctly functioning SAWR, and the circuit will begin to oscillate.

## 10 MHz Reference

The spectrum analyzer 10 MHz reference consists of 10 MHz OCXO (Option 103: TCXO) with associated TTL level generator and distribution circuitry. The OCXO (or TCXO) and TTL level generator are turned off when an external 10 MHz reference is used. Also, with the spectrum analyzer set to EXTERNAL frequency reference, U304A output (low) forces the output of U304D to stay high. This allows U304B to control the outputs of U303B, U304C, and U303D. In INTERNAL frequency reference, U304D controls the outputs of these three NAND gates, and the output of U304B is held high.

Check the 10 MHz reference by performing the following steps:

1. Set the HP 8560E's 10 MHz reference to internal by pressing **AUX CTRL**, **REAR PANEL**, and **10 MHz INT**.

hp running

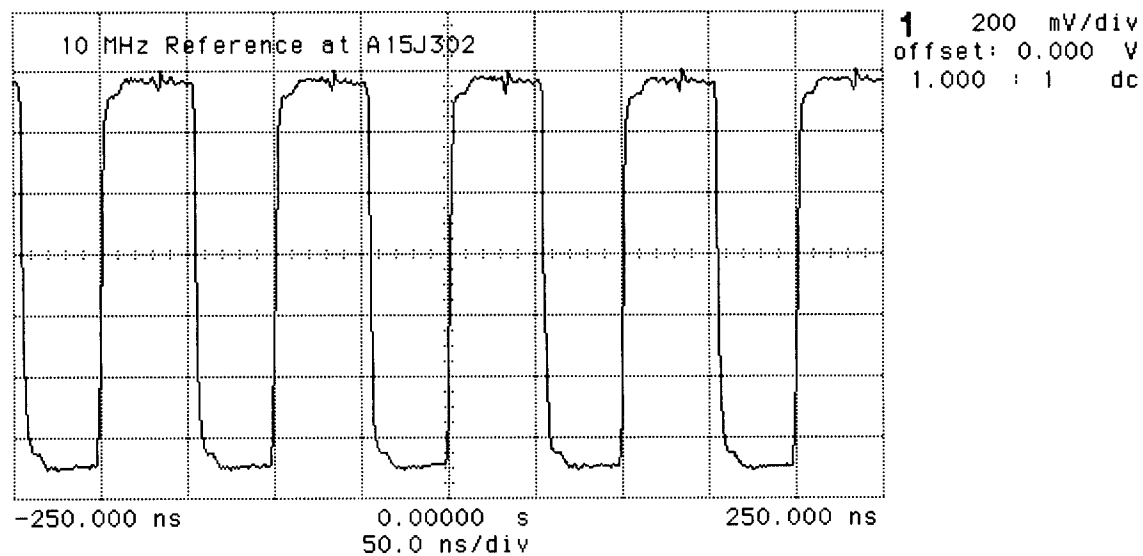


Figure 11-3. 10 MHz Reference at A15J302

hp stopped

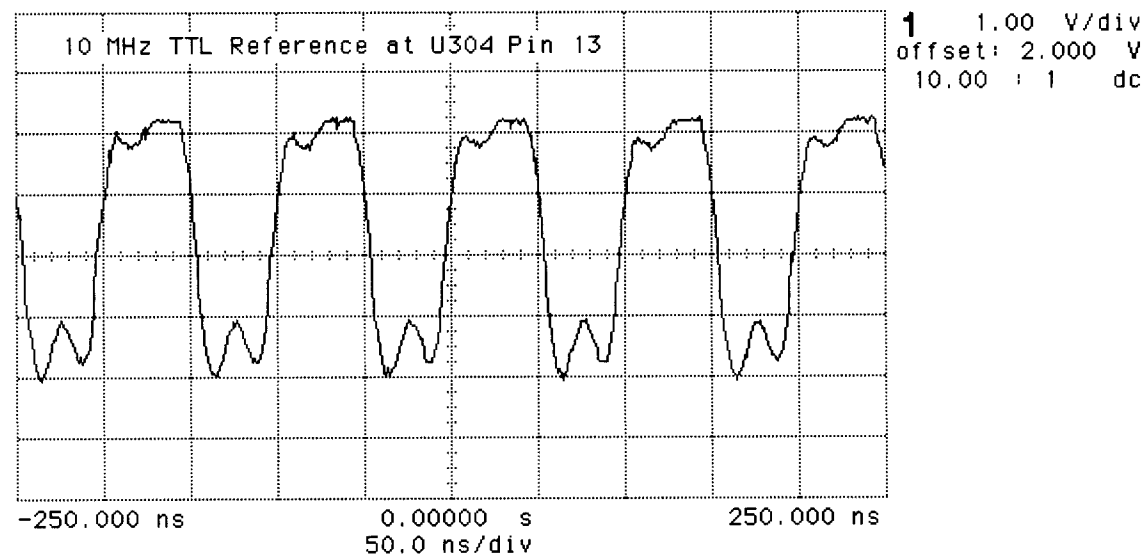


Figure 11-4. 10 MHz TTL Reference at U304 Pin 13

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## **A10 Tracking Generator (Option 002)**

### **Block Diagram Description**

The A10 tracking generator consists of several smaller circuits. The A10 is not component-level repairable; a rebuilt exchange assembly is available.

The block diagram of the tracking generator is unique in that it only recreates one of the spectrum analyzer's intermediate frequencies. This minimizes isolation problems associated with a built-in tracking generator. Each of the blocks comprising the A10 tracking generator is described below.

### **Tracking Oscillator**

The tracking oscillator enables the fine adjustment of the tracking generator output frequency to compensate for the frequency inaccuracies of the spectrum analyzer's 10.7 MHz IF. The tracking oscillator determines the residual FM and frequency drift of the tracking generator. The 182.14 MHz output frequency is obtained by doubling the output of a crystal oscillator operating at 91.07 MHz.

### **Upconverter**

The upconverter mixes the tracking oscillator output with the buffered 600 MHz reference from the A15 RF assembly. The upconverter also contains a filter to pass only the 782.14 MHz upper sideband.

### **Pentupler**

The pentupler multiplies the 782.14 MHz signal by five to generate 3.9107 GHz, the spectrum analyzer's 1st IF. A dual cavity band-pass filter centered at 3.9107 GHz eliminates all unwanted multiples of 782.14 MHz.

### **Modulator**

The output of the pentupler is passed through a modulator to adjust the power level into the output mixer. The modulator is controlled by an ALC circuit on the bias board which is fed by a detector in the output amplifier. If the detected output power is too high, the ALC will drive the Modulator to decrease the input level into the output mixer, resulting in a decrease in output power.

### **Coupler**

The 1st LO signal from the A7 LODA is coupled off and buffered to drive the output mixer. The main line of the coupler is fed to the 1ST LO OUTPUT on the front panel. The loss through the coupler main line is less than 2.5 dB.

### **Output Mixer**

The 3.9107 GHz signal from the modulator is fed into the RF port of the output mixer. The LO port of the output mixer is driven by the buffered 1st LO signal from the coupler. The output of the mixer is then amplified.

3. Check maximum power available from the TG. Connect the RF OUT 50 $\Omega$  to the INPUT 50 $\Omega$  connector. Press **PRESET**, **AMPLITUDE**, **2**, **0**, **+ dBm**, **LOG dB/DIV**, **5**, **dB**, **AUX CTRL**, **TRACKING GENERATOR**, **SRC PWR ON**, **MORE 1 OF 3**, **ALC EXT**. No connection should be made to the ALC EXT INPUT connector on the rear panel. The available power should always be greater than +1 dBm. If the output is unleveled only at specific frequencies, a power hole will usually be visible at those frequencies.
4. Perform the "1ST LO OUTPUT Amplitude" performance test. If the test fails, note the center frequency setting at which the power level was out-of-tolerance. Repeat the test with the power sensor connected to A7J3 (a right-angle SMA adapter will be necessary) and note the center frequency of any out-of-tolerance power levels. The power level should be +16.5 dBm  $\pm$  2 dB.  
  
If the power level is correct at W43 but out-of-tolerance at the 1ST LO OUTPUT (front panel) and the center frequency setting of the out-of-tolerance power levels is close to the frequencies at which the output is unleveled, suspect either A10 or W46.  
  
If the power level at W43 is also out-of-tolerance, suspect either the A7 LODA or the A11 YTO. Refer to Chapter 10, "Synthesizer Section."
5. If the output is unleveled only at certain power level settings or certain frequencies, monitor A17J16 pin 1 with a DVM. Connect the negative DVM lead to A17J16 pin 6. Vary the TRK GEN RF POWER or center frequency settings, as appropriate, and plot the voltage variation versus power level or frequency. A discontinuity in the plot near the frequency or power level at which the output is unleveled indicates a problem on the A14 frequency control assembly.

## Excessive Residual FM

Either the tracking oscillator or the ALC circuitry could be responsible for excessive residual FM. The residual FM should be measured on another spectrum analyzer, such as an HP 8566A/B or HP 8568A/B, using slope detection with the HP 8560E set to zero span.

Proceed as follows to troubleshoot residual FM problems:

1. Perform the "Residual FM" performance test for the spectrum analyzer in the *HP 8560 E-Series Spectrum Analyzer Calibration Guide*. If this test passes, the 1st LO input and 600 MHz drive signals should be correct. If the test fails, troubleshoot the synthesizer section.
2. Monitor A14J17 pin 15 (TUNE +) with an oscilloscope. Connect the oscilloscope probe ground lead to A14J17 pin 6. The voltage at this point should be greater than 500 mV. If the voltage is less than 500 mV, perform the "Tracking Oscillator Range" performance test in the *HP 8560 E-Series Spectrum Analyzer Calibration Guide*. If this test fails, perform the "Tracking Oscillator Range Adjustment". If the noise on this tune line is greater than 10 mV, troubleshoot the BITG drive circuitry on A14.
3. Monitor the output of the tracking generator with another spectrum analyzer. Check for high-amplitude spurious responses from 100 kHz to at least 3 GHz. If the spurious responses are too high in amplitude, the (broadband) ALC detector may cause the ALC loop to oscillate, generating FM sidebands. If any spurious responses are excessively high, refer to "Harmonic/Spurious Outputs Too High" in this chapter.
4. If no spurious responses are present or are sufficiently low enough in amplitude to not cause a problem, suspect the tracking oscillator in A10.

3. Check for excessive LO feedthrough. Use the “LO Feedthrough” performance test in the *HP 8560 E-Series Spectrum Analyzer Calibration Guide*, but check over a center frequency range of 300 kHz to 100 MHz. The LO feedthrough will be 3.9107 GHz greater than the center frequency setting.

### Harmonic/Spurious Outputs Too High

Harmonic and spurious outputs may be generated by A10 itself or may be present on the either the 600 MHz drive or 1st LO drive signal. There is a direct relationship between spurious signals on the 1st LO and spurious signals on the TG output. There is a five-to-one relationship between spurious signals on the 600 MHz drive and the spurious signals on the TG output. For example, if the 600 MHz signal moves 1 MHz, the TG output signal will move 5 MHz. This is due to the multiplication in the pentupler.

1. If the “Harmonic Spurious Responses” performance test failed, connect another spectrum analyzer, such as an HP 8566A/B, to the HP 8560E 1ST LO OUTPUT connector. Set the HP 8560E to each frequency as indicated in the performance test, with the span set to 0 Hz. At each frequency setting, press **SGL SWP**, **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, **LO FREQ**. The frequency displayed will be the fundamental frequency of the 1ST LO OUTPUT. Use the HP 8566A/B to measure the level of the second and third harmonics of the 1st LO signal.

---

|             |                                                                                                                                                                                                     |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note</b> | The 1st LO typically has a higher harmonic content than the tracking generator output. For the purposes of this check, it is the variation in harmonic content versus frequency which is important. |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

---

If the variation of the harmonic level of the 1st LO versus frequency tracks the harmonic level variation of the tracking generator output, repeat this step while measuring the 1st LO signal at the end of W43 nearest A10. If there is little variation in the 1st LO harmonic level between the 1ST LO OUTPUT connector and W43, and the relative variation in harmonic level tracks with the TG output harmonic level, suspect either the A7 LODA or A11 YTO.

If the harmonic level variation of the 1st LO versus frequency does not track the harmonic level variation of the TG output, suspect A10.

2. If sidebands are present at the same frequency offset at every output frequency, check the spectral purity of the 1st LO and the 600 MHz drive signals using another spectrum analyzer. When checking the 1st LO, the HP 8560E must be set to zero span. Press **CAL**, **MORE 1 OF 2**, **FREQ DIAGNOSE**, **LO FREQ** to determine the 1st LO frequency. A 1 MHz sideband on the 1st LO will appear as a 1 MHz sideband on the output signal.

To verify that the 600 MHz drive or 1st LO signal is responsible for the sidebands, substitute a clean signal for the 600 MHz drive or 1st LO signal. If the sidebands on the output disappear when using the clean signal, the substituted signal was responsible for the sidebands.

---

|             |                                                                                                         |
|-------------|---------------------------------------------------------------------------------------------------------|
| <b>Note</b> | The 600 MHz drive signal should be -8 dBm $\pm$ 3.5 dB. The 1st LO signal should be +16 dBm $\pm$ 2 dB. |
|-------------|---------------------------------------------------------------------------------------------------------|

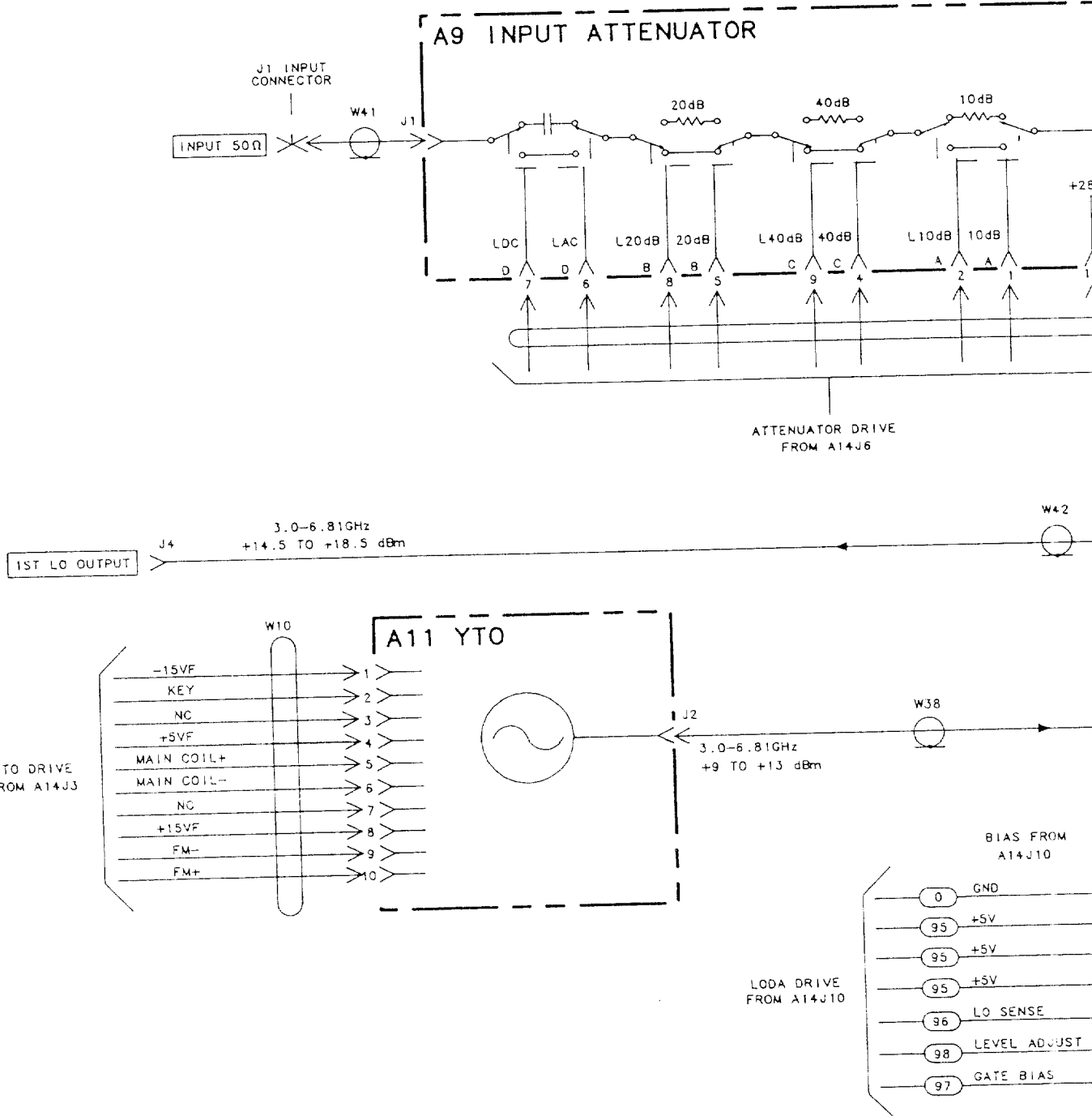
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7. If all of the checks above are correct, the tracking oscillator might not be functioning. Setup the HP 8560E as indicated in the "Tracking Oscillator Range Adjustment" procedure, using a spectrum analyzer, such as an HP 8566A/B, in place of the frequency counter. Try to adjust A10C3 until a signal is displayed on the HP 8566A/B. If adjusting A10C3 does not start the tracking oscillator functioning, suspect the A10 tracking generator.

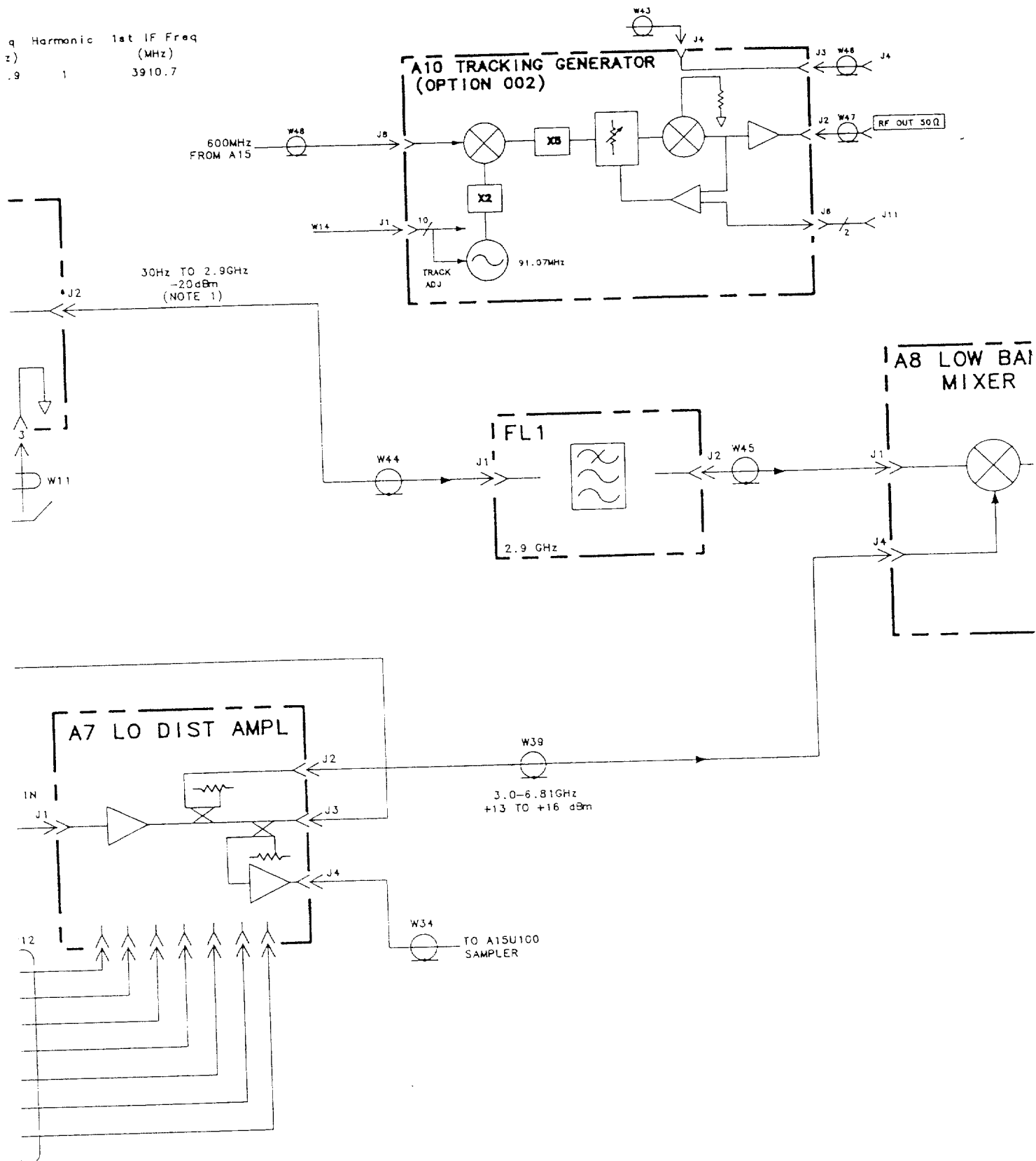
# RF SECTION BLOCK DIAGRAM

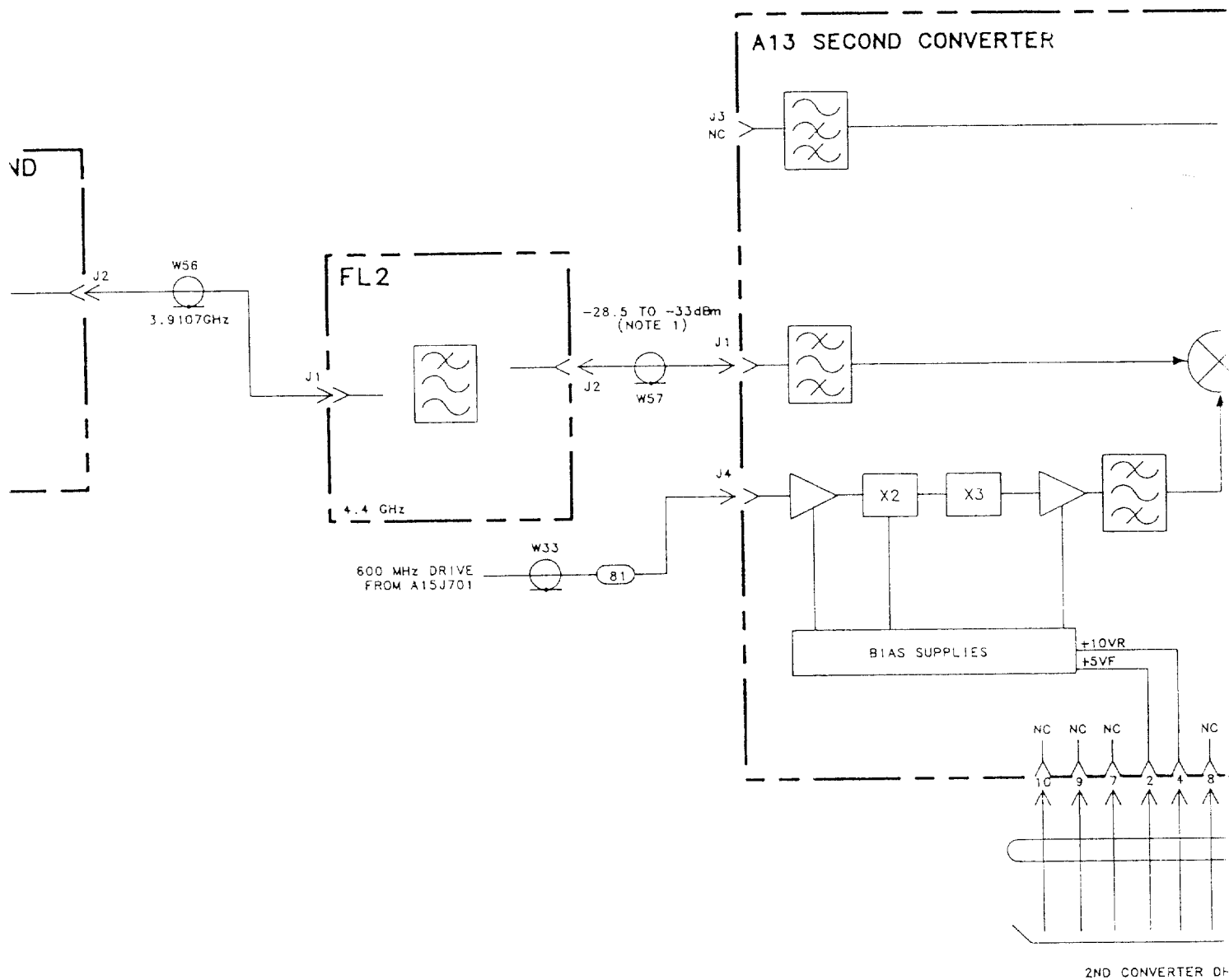
Band

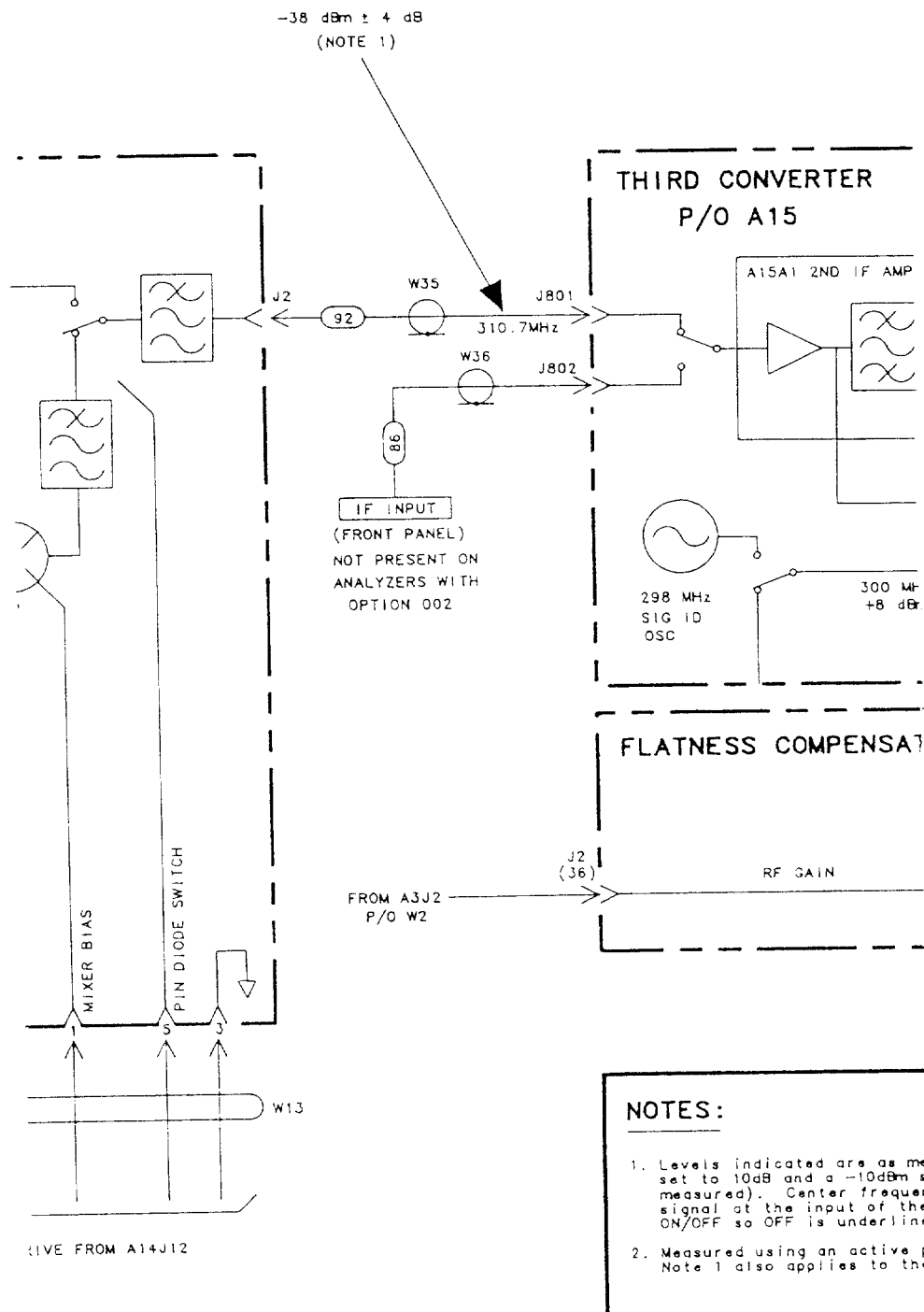
0

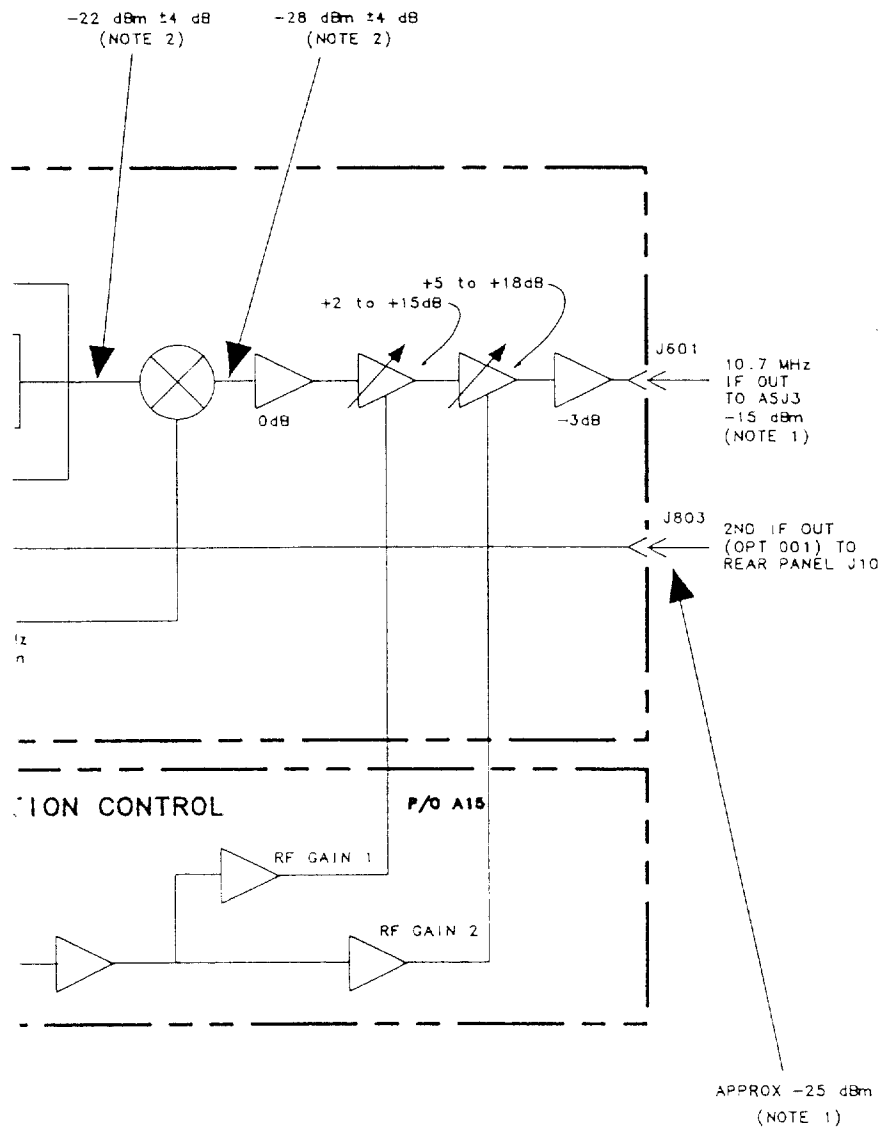


q Harmonic 1st IF Freq  
 z) (MHz)  
 .9 1 3910.7









measured with the HP 8560E input attenuation signal level at the INPUT (in the band being measured) must be tuned to the frequency of the HP 8560E. Press SPAN, 0Hz, then CAL, IF ADJ. Press SGL SWP.

probe and an additional spectrum analyzer. see levels.

FIGURE 11-5. RF SECTION, TROUBLESHOOTING BLOCK DIAGRAM

## Display/Power Supply Section

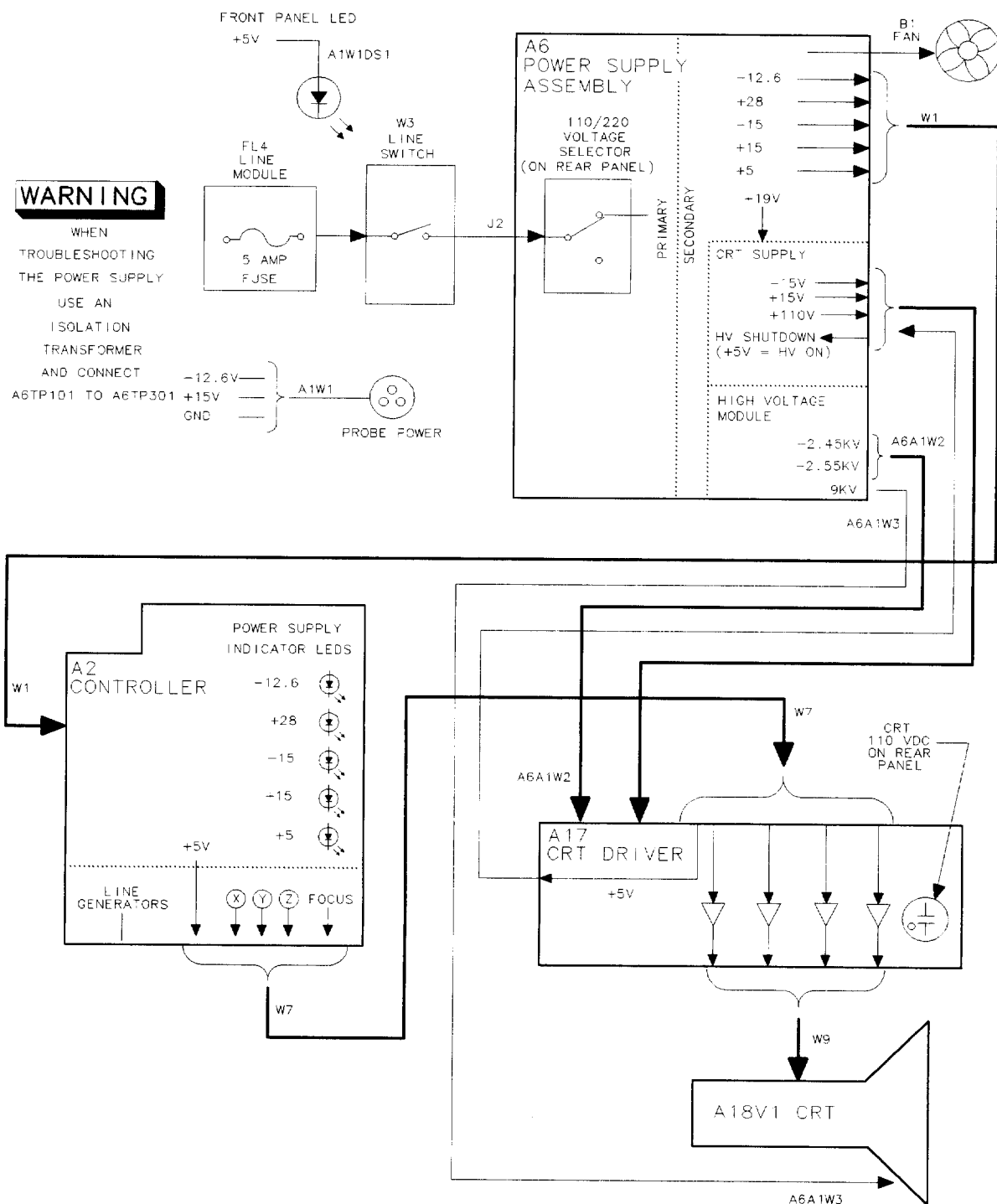
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The display/power supply section contains the A6 power supply, A6A1 HV module, A17 CRT driver, and A18 CRT. Figure 12-1 illustrates the section block diagram. Table 12-1 lists signal versus pin numbers for power cable W1.

- Troubleshooting Using the TAM
  - Blank Display (Using the TAM)
- Blank Display
- Blanking Signal
- Display Distortion
- Focus Problems
- Intensity Problems
- A6 Power Supply Assembly
  - Dead Power Supply
  - Line Fuse Blowing
  - Supply Restarting Every 1.5 Seconds (Kick Start)
  - Low Voltage Supplies
  - High Voltage Supplies
  - CRT Supply Dropping Out
  - Blanking Signal
  - Buck Regulator Control
  - DC-DC Converter Control
  - Power Up

### Warning

- The A6 power supply and A6A1 high voltage assemblies contain lethal voltages with lethal currents in all areas. Use extreme care when servicing these assemblies. Always disconnect the power cord from the instrument before servicing these assemblies. Failure to follow this precaution can represent a shock hazard which may result in personal injury.
- The voltage potential at A6A1W3 is +9 kV. If the cable must be disconnected, always disconnect it at the CRT with caution! Failure to properly discharge A6A1W3 may result in severe electrical shock to personnel and damage to the instrument. See procedure 2 in Chapter 3.
- Do not discharge the CRT second anode directly to ground, with the A6A1 high voltage cable connected. This can damage the A17 CRT driver assembly. Always discharge through a high resistance, such as a high voltage probe.
- Always use an isolation transformer when troubleshooting either the A6 power supply or the A6A1 HV module. When using an isolation transformer, connect a jumper between A6TP101 and A6TP301. This connects the circuit common to earth ground. Remove this jumper when the isolation transformer is not used.



sp141e

Figure 12-1. Simplified Power Supply Block Diagram

## 12-2 Display/Power Supply Section

**Table 12-1. W1 Power-Cable Connections**

| Signal    | A2J1<br>(pins) | A3J1<br>(pins) | A4J1<br>(pins) | A5J1<br>(pins) | A6J1-<br>(pins) | A14J1<br>(pins) | A15J1<br>(pins) |
|-----------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|
| NC        | -              | -              | -              | -              | -               | -               | -               |
| NC        | -              | -              | -              | -              | -               | -               | -               |
| A GND     | -              | 3              | 3              | 48             | 3*              | 3               | 3               |
| NC        | -              | -              | -              | -              | -               | -               | -               |
| NC        | -              | -              | -              | -              | -               | -               | -               |
| A GND     | -              | 6              | 6              | 45             | 6*              | 6               | 6               |
| NC        | -              | -              | -              | -              | -               | -               | -               |
| NC        | -              | -              | -              | -              | -               | -               | -               |
| A GND     | -              | 9              | 9              | 42             | 9*              | 9               | 9               |
| SCAN RAMP | 41             | 10             | -              | -              | -               | 10*             | -               |
| NC        | -              | -              | -              | -              | -               | -               | -               |
| A GND     | -              | 12             | 12             | 39             | 12*             | 12              | 12              |
| -12.6 V   | 38             | 13             | -              | -              | 13*             | -               | -               |
| -15 V     | -              | 14             | 14             | 37             | 14*             | 14              | 14              |
| A GND     | -              | 15             | 15             | 36             | 15*             | 15              | 15              |
| -15 V     | -              | 16             | 16             | 35             | 16*             | 16              | 16              |
| +15 V     | -              | 17             | 17             | 34             | 17*             | 17              | 17              |
| A GND     | -              | 18             | 18             | 33             | 18*             | 18              | 18              |
| +15 V     | -              | 19             | 19             | 32             | 19*             | 19              | 19              |
| +28 V     | -              | 20             | -              | -              | 20*             | 20              | 20              |
| +28 V     | -              | 21             | -              | -              | 21*             | 21              | 21              |
| PWR UP    | 29             | -              | -              | -              | 22*             | -               | -               |
| -15 V     | -              | 23             | 23             | 28             | 23*             | 23              | 23              |
| -15 V     | -              | 24             | 24             | 27             | 24*             | 24              | 24              |
| +15 V     | -              | 25             | 25             | 26             | 25*             | 25              | 25              |
| +15 V     | -              | 26             | 26             | 25             | 26*             | 26              | 26              |
| +5 V      | -              | 27             | 27             | 24             | 27*             | 27              | 27              |
| +5 V      | -              | 28             | 28             | 23             | 28*             | 28              | 28              |
| +5 V      | -              | 29             | 29             | 22             | 29*             | 29              | 29              |
| +5 V      | -              | 30             | 30             | 21             | 30*             | 30              | 30              |
| D GND     | 20             | 31             | 31             | 20             | 31*             | -               | 31              |
| D GND     | 19             | 32             | 32             | 19             | 32*             | -               | 32              |
| A GND     | 18             | 33             | 33             | 18             | 33*             | 33              | 33              |
| A GND     | 17             | 34             | 34             | 17             | 34*             | 34              | 34              |
| D GND     | 16             | 35             | 35             | 16             | 35*             | 35              | 35              |
| D GND     | 15             | 36             | 36             | 15             | 36*             | 36              | 36              |
| D GND     | 14             | 37             | 37             | 14             | 37*             | 37              | 37              |
| D GND     | 13             | 38             | 38             | 13             | 38*             | 38              | 38              |

**Table 12-1. W1 Power-Cable Connections (continued)**

| Signal                                | A2J1<br>(pins) | A3J1<br>(pins) | A4J1<br>(pins) | A5J1<br>(pins) | A6J1-<br>(pins) | A14J1<br>(pins) | A15J1<br>(pins) |
|---------------------------------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|
| +5 V                                  | 12             | 39             | -              | -              | 39*             | -               | -               |
| +5 V                                  | 11             | 40             | -              | -              | 40*             | -               | -               |
| +5 V                                  | 10             | 41             | -              | -              | 41*             | -               | -               |
| +5 V                                  | 9              | 42             | -              | -              | 42*             | -               | -               |
| +5 V                                  | 8              | 43             | -              | -              | 43*             | -               | -               |
| +5 V                                  | 7              | 44             | -              | -              | 44*             | -               | -               |
| +28 V                                 | 6              | 45             | -              | -              | 45*             | -               | -               |
| LINE TRIGGER                          | -              | 46             | -              | -              | 46*             | -               | -               |
| +15 V                                 | 4              | 47             | -              | -              | 47*             | -               | -               |
| +15 V                                 | 3              | 48             | -              | -              | 48*             | -               | -               |
| -15 V                                 | 2              | 49             | 49             | -              | 49*             | -               | -               |
| -15 V                                 | 1              | 50             | 50             | -              | 50*             | -               | -               |
| * Indicates signal source connectors. |                |                |                |                |                 |                 |                 |

## Troubleshooting Using the TAM

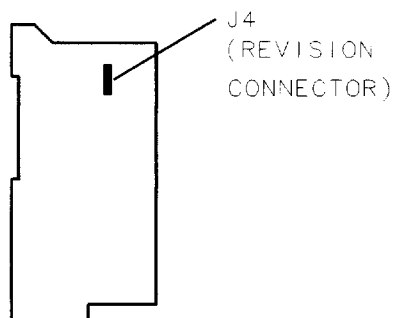
When using automatic fault isolation, the TAM indicates suspected circuits that need to be manually checked. Use Table 12-2 to locate the manual procedure.

Table 12-3 lists assembly test connectors associated with each manual probe troubleshooting test. Figure 12-2 illustrates the location of A17's test connectors.

**Table 12-2. Automatic Fault Isolation References**

| Suspected Circuit Indicated<br>by Automatic Fault Isolation | Manual Procedure to Perform              |
|-------------------------------------------------------------|------------------------------------------|
| Check A2 Controller                                         | Blanking Signal                          |
| Check All Power Supply Outputs                              | Dead Power Supply ( <i>steps 1-5</i> )   |
| Check Buck Regulator                                        | Dead Power Supply ( <i>steps 13-23</i> ) |
| Check Buck Regulator Control Circuitry                      | Dead Power Supply ( <i>steps 11-21</i> ) |
| Check High-Voltage Supplies                                 | High Voltage Supplies                    |
| Check Input Rectifier                                       | Dead Power Supply ( <i>steps 6-7</i> )   |
| Check Intensity Adjustments                                 | Intensity Problems ( <i>steps 1-4</i> )  |
| Check Kick Start/Bias Circuitry                             | Dead Power Supply ( <i>steps 8-10</i> )  |
| Check Low-Voltage Supplies                                  | Low Voltage Supplies                     |

# A17 CRT DRIVER



SK 1121

**Figure 12-2. A17 Test Connector**

**Table 12-3. TAM Tests versus Test Connectors**

| Connector | Manual Probe Troubleshooting Test | Measured Signal Lines |
|-----------|-----------------------------------|-----------------------|
| A17J4     | Revision                          | MS5                   |
|           | Constant current Source           | MS1                   |
|           | Intensity input                   | MS7                   |
|           | Intensity offset                  | MS7                   |
|           | Blanking control                  | MS8                   |
| A2J201    | 10 V reference test               | MS4                   |
|           | Switch drive test                 | MS3                   |
|           | Buffered X & Y DAC outputs        | MS2, MS7              |
|           | X line generator test             | MS6                   |
|           | Y line generator test             | MS1                   |
|           | Intensity offset output           | MS8                   |
| A2J202    | Revision                          | MS1                   |
|           | X, Y, & Z output offset           | MS3, MS4, MS7         |
|           | X output amplifier                | MS7                   |
|           | Y output amplifier                | MS3                   |
|           | Blanking test                     | MS4                   |
|           | Focus DAC test                    | MS2                   |

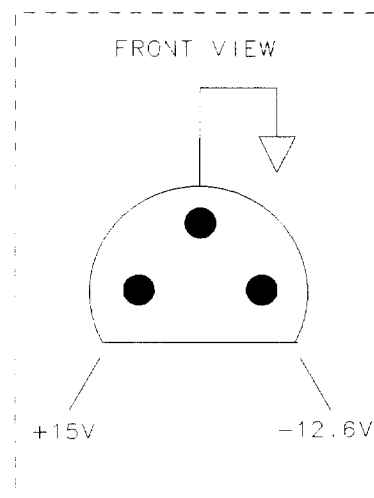
## Blank Display (Using the TAM)

Use the following procedure if the instrument's display is blank. This procedure substitutes an HP-IB printer for the display.

1. Connect the printer to the HP 8560E spectrum analyzer and set the printer's address to the value required by the TAM. This is usually 1.
2. All of the power-supply indicator LEDs along the edge of the A2 controller assembly should be lit.
3. The rear-panel CRT +110 VDC ON indicator should also be lit.
4. Connect the TAM's probe cable to A2J11.
5. Press **MODULE**, **SOFT KEY #3**, **▼**, and **SOFT KEY #1**. (The top soft key is #1.)
6. The yellow LED next to A2J11 should blink approximately ten times. If the LED fails to blink correctly, troubleshoot the digital section of the A2 controller assembly.
7. Move the probe cable to A2J202. Press **SOFT KEY #1** and wait 5 seconds.
8. Press **SOFT KEY #4**. The results should be sent to the printer.
9. Move the probe cable to A2J201, press **SOFT KEY #1** and wait 5 seconds.
10. Press **SOFT KEY #4**. The results will be sent to the printer.
11. If a failure is indicated in any of these tests, the fault lies on the A2 controller assembly. to obtain more information:
  - a. Press the down arrow key one less time than the test number. (For example, press it twice for the third test on the list.)
  - b. Press **SOFT KEY #3**, then **SOFT KEY #4**, and when the printout is complete, **SOFT KEY #6**.
12. If no failures were indicated in testing the A2 controller, move the probe cable to A17J4.
13. Press **SOFT KEY #1** and wait 5 seconds.
14. Press **SOFT KEY #4**. The results will be sent to the printer.
15. If no failure is indicated in the printout, check the high-voltage supplies as described "High Voltage Supplies" in this chapter.

## Blank Display

1. If the LED above the front-panel LINE switch is lit, most of the A6 power supply is functioning properly.
2. Carefully check the voltages on the front-panel PROBE POWER jack. Be careful to avoid shorting the pins together. See Figure 12-3.
3. Check that the fan is operating. If the PROBE POWER voltages are correct, and the fan is turning, the A6 power supply is probably working properly.
4. If the rear-panel's CRT +110 VDC ON LED is lit, the high-voltage supplies should also be operating. (The high-voltage supplies will be turned off if the HV SHUT\_DOWN line is low.) The A6 power supply feeds +5 V to the A2 controller through W1. The A2 assembly distributes this +5 V to the A17 CRT driver through W7. A17 sends +5 V back to A6 as the HV SHUT\_DOWN signal on W8. As a result, A2, A17, W1, W7, and W8 must all be in place for the high-voltage supplies to operate.
5. If all of the power supply indicators along the outside edge of the A2 controller assembly are lit, the A6 power supply is probably working properly.



SK 1122

**Figure 12-3. Probe Power Socket**

6. Press **FREQUENCY**, 1, **GHz**.
7. Allow the analyzer to warm-up for at least 1 minute.
8. While observing the display, press **LINE** to turn the spectrum analyzer off. If a green flash appears on the display, the CRT is probably working properly; troubleshoot either the A2 controller or the A17 CRT driver.
9. If a flash does not appear on the display, the A2 controller, A6A1 HV module, A17 CRT driver, or A18V1 CRT might be at fault.

---

## Blanking Signal

1. Connect an oscilloscope probe to A2J202 pin 3. Connect the oscilloscope ground lead to TP3. Set the oscilloscope to the following settings:

Sweep time ..... 2 ms/div  
Vertical scale ..... 1 V/div

2. If a 4 Vp-p signal is not observed, the A2 controller assembly is faulty.

3. Repeat steps 1 and 2 with the oscilloscope probe on A2J202 pin 14.

4. Set the oscilloscope to the following settings:

Sweep time ..... 1  $\mu$ s/div  
Vertical scale ..... 2 V/div

5. Connect the positive probe lead to A2J202 pin 15. This is the blanking output.

6. TTL-level pulses should be observed. If the signal is either always high or always low, the display will be blanked; suspect the A2 controller assembly.

7. If the signals on A2J202 pins 3, 14, and 15 are correct, troubleshoot the A17 CRT driver.

---

## Display Distortion

The HP 8560E uses a vector display. The graticule lines, traces, and characters are composed of a series of straight lines (“vectors”) placed end-to-end. If the vectors do not begin and end at the proper points, the display appears distorted, but in focus. Symptoms range from characters appearing elongated and graticule lines not meeting squarely, to an entirely unreadable display.

1. If the spectrum analyzer is in external frequency reference mode (an “X” is displayed along the left side of the display), ensure that an external 10 MHz reference is supplied. Otherwise the 16 MHz CPU clock will be off-frequency, causing distortion.
2. Use the CRT ADJ PATTERN to check for distortion. Press **CAL**, **MORE 1 OF 2**, and **CRT ADJ PATTERN**. If vector distortion (described above) occurs, perform the “Display Adjustment” in Chapter 2 to test the function of the A2 controller assembly.
3. If there is distortion along with slight focus degradation, but the graticule lines meet (not necessarily squarely), the A17 CRT driver, CRT, DDD/TRACE ALIGN adjustments, or cable connections might be at fault.
4. If the A2 controller assembly is not part number 08563-60017, perform the “16 MHz PLL adjustment” in Chapter 2. If the 16 MHz CPU clock is off-frequency, the display will be distorted.
5. Perform the “Display Adjustment” in Chapter 2. Isolate the problem to either the X or Y axis by noting the behavior of the adjustments. If the line generator or fast zero-span portion of the adjustment fails, troubleshoot the A2 controller assembly.
6. If the adjustments do not remedy the problem, press **LINE** to turn the spectrum analyzer off and place the A17 CRT driver in the service position.

7. Distortion confined to one axis (vertical or horizontal only), indicates a faulty A17 assembly's X or Y deflection amplifier. Use the alternate good deflection amplifier for obtaining typical voltages. (There is enough symmetry in a typical display that the voltages should be similar between these circuits.)
8. Monitor the waveforms at A17TP11 and A17TP14 (or TP12 and TP13). The 50 to 100 Vp-p ac component of the waveforms at the X and  $\bar{X}$  (or Y and  $\bar{Y}$ ) outputs should be mirror images of each other. The dc average should be 55 V.
9. The appropriate POSN adjustment (A17R57 or A17R77) should change the dc component of both X and  $\bar{X}$  (or Y and  $\bar{Y}$ ) outputs in opposite directions.
10. The appropriate GAIN adjustment (A17R55 or A17R75) should change the ac component in both outputs by the same amount.
11. If the display is a single dot, check the base of A17Q18 for  $-10.3 \text{ V} \pm 0.3 \text{ V}$ . Verify the signals at TP11, TP14, TP12, and TP13.
12. If signals are correct and cables to the CRT are good, suspect the CRT.

---

## Focus Problems

Focus problems may be due to a defective A18V1 CRT, the A17 CRT driver (especially the grid level shifter section), or the A2 controller's focus-control circuitry. Focus problems may also be due to improper adjustments, improper connections, or absence of high voltage.

Although A17's grid level shifter (function block D) is the leading cause of A17 focus problems, function blocks C, E, F, and H generally have less effect on focus, but may cause poor focus that is a function of screen position, length of line, or intensity.

1. Connect a DVM's positive lead to A2J202, pin 2. Connect the negative lead to A2J202 pin 6.
2. Use the knob to change the focus DAC value from 0 to 255.
3. If the DVM reads near 0 Vdc with the focus set to 0, and near  $-10 \text{ Vdc}$  with the focus set to 255, A2's focus control circuitry is working properly.
4. Perform the "Display Adjustment" in Chapter 2. Note that A17R34 COARSE FOCUS has the greatest effect on focus. Adjustment A17R93 ASTIG and A17R92 DDD have a lesser effect, and A17R21 Z FOCUS, A17R26 X FOCUS and front-panel adjustment (press **DISPLAY**, **MORE 1 OF 2**, **FOCUS**, and turn knob) have less effect on focus.
5. If the focus of some areas of the screen are worse than normal, continue with step 11. If no part of the screen can be brought to sharp focus, continue with step 6. (CRTs have some normal focus variation across their face.)
6. Turn off the analyzer and place A17 in the service position. Connect the ground lead of a high-voltage probe (HP 34111A) to the chassis, and use it with a DVM to measure A17J7(10).

7. The nominal A17J7(10) voltage is  $-1600\text{ Vdc}$ , but the CRT will function if this voltage is within  $200\text{ V}$  of  $-1600\text{ Vdc}$ .
8. Adjusting A17R34 COARSE FOCUS should vary the A17J7(10) voltage by  $150\text{ V}$ . If these voltages are correct, suspect the CRT.
9. Check the A6A1 high voltage module cathode supply output at A17TP16 using a high voltage probe. If the cathode voltage is  $-2450\text{ V} \pm 250\text{ V}$ , check the focus grid level shifter.
10. If the cathode voltage is not correct, check the A6A1 high voltage module and its connections.
11. Connect an oscilloscope probe to A17TP9. This signal corrects the focus for the X position of the CRT beam, and for intensity level. It also provides the front-panel focus adjusting voltage.
12. Press **DISPLAY**, **MORE 1 OF 2**, and **FOCUS**. While turning the front-panel knob, verify the dc level of the signal at TP9 adjusts about  $30\text{ Vp-p}$ .
13. Verify that the front panel intensity adjustment, when used with the A17R21 Z FOCUS, changes the peak-to-peak voltage at TP9 by  $25\text{ V}$ . Access the intensity adjustment by pressing **DISPLAY**, **INTENSITY**, and turning the front panel knob.
14. Set front panel intensity to minimum. Set A17R21 Z FOCUS and A17R26 X FOCUS fully counterclockwise. Verify that the peak-to-peak voltage at TP9 is about  $40\text{ Vp-p}$  (due to X-dynamic focus circuit).
15. If circuit operation seems correct, the A18V1 CRT is probably at fault.

---

## Intensity Problems

Intensity problems, or absence of display, can be due to the A17 assembly's intensity amplifier (function block A), intensity grid level shifter (function block B), CRT (A18V1), interconnections, or lack of proper supplies or inputs to A17.

1. On the HP 8560E spectrum analyzer press **DISPLAY** and **INTENSITY**.
2. Rotate the front-panel knob (RPG), and check that the intensity changes from dim, but readable, to bright.
3. If the intensity function does not function properly, troubleshoot the A2 controller assembly.
4. Perform the preliminary and Z-axis portions of the "Display Adjustment" in Chapter 2. Verify that A17R11 CUTOFF functions properly. If A17R11 CUTOFF does not function properly, place the A17 CRT driver in the service position.
5. Verify that blanking pulses are present at A17TP2 using an oscilloscope. The pulses should be normal TTL levels, approximately  $1\text{ }\mu\text{s}$  wide and  $4$  or  $7\text{ }\mu\text{s}$  apart. If the blanking pulses are not correct, check the BLANKING output of the A2 controller assembly and cable W7.

6. If blanking pulses are present, check A17TP10 with the oscilloscope. The TP10 signal should vary with the front-panel intensity adjustment, and be approximately 55 Vp-p maximum. The signal will be composed of both blanking pulses and varying intensity levels for the lines being drawn.
  - a. If a proper signal is not present at A17TP10, check A17Q1, Q2, CR1, and CR2.
  - b. If the TP10 signal does not vary with the front-panel intensity adjustment, check the signals at A17TP4 and A17TP1. Both signals should vary with the front panel intensity adjustment. The TP4 signal should be up to 4 Vp-p, and the TP1 signal should be up to approximately 12 Vp-p.

---

|                |                                                                                                                                                                                                                                                                                                                |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Warning</b> | <b>The A17 CRT Driver contains lethal voltages with lethal currents. Use extreme care when servicing this assembly. Always disconnect the power cord from the instrument before servicing this assembly. Failure to follow this precaution can present a shock hazard which may result in personal injury.</b> |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

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|             |                                                                                                                                                                                          |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note</b> | The following measurements should be made with a high-voltage probe, such as the HP 34111A. When using the high-voltage probe, connect the ground lead securely to the HP 8560E chassis. |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

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7. Carefully measure the grid voltage at A17J7 pin 6, and the cathode voltage at A17J7 pin 4. The display will work with a cathode voltage of  $-2450\text{ V} \pm 250\text{ V}$ , provided the grid voltage (A17J7 pin 6) is 30 to 100 V more negative than the cathode. A17R11, CUTOFF, should be able to adjust the voltage difference over a 60 V range to account for tube variations, and achieve proper intensity.
8. If the grid and cathode voltages are correct, turn off the HP 8560E spectrum analyzer and check A17CR10 with an ohmmeter. If A17CR10 is good, suspect the A18V1 CRT.
9. If the grid and cathode voltages are too low, turn off the power and disconnect W8 from the base of A18V1 CRT, and recheck the grid and cathode voltages.
10. If the grid and cathode voltages are still too low, refer to "CRT Supply" in this chapter and the "High-Voltage Power Supply Adjustment" procedure in Chapter 2.
11. If voltages are correct when the tube is disconnected, the CRT is probably defective.

---

|                |                                                                                                 |
|----------------|-------------------------------------------------------------------------------------------------|
| <b>Caution</b> | The pins on the A18V1 CRT bend easily. Be careful not to bend pins when connecting W8 to A18V1. |
|----------------|-------------------------------------------------------------------------------------------------|

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## A6 Power Supply Assembly

The HP 8560E spectrum analyzer uses a switching power supply operating at 40 kHz to supply the low voltages for most of the analyzer hardware and a 30 kHz switching supply (CRT supply) to provide the high voltages for the CRT display. The CRT supply will be treated as a separate supply since the remainder of A6 must be operating for the CRT supply to operate.

Kick starting occurs when there is a fault either on the power supply or on one of the other assemblies. The power supply will try to start by generating a 200 ms pulse (“kick”) every 1.5 seconds. A kick-starting power supply often appears to be dead, but the fan will make one or two revolutions and stop every 1.5 seconds.

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### Warning

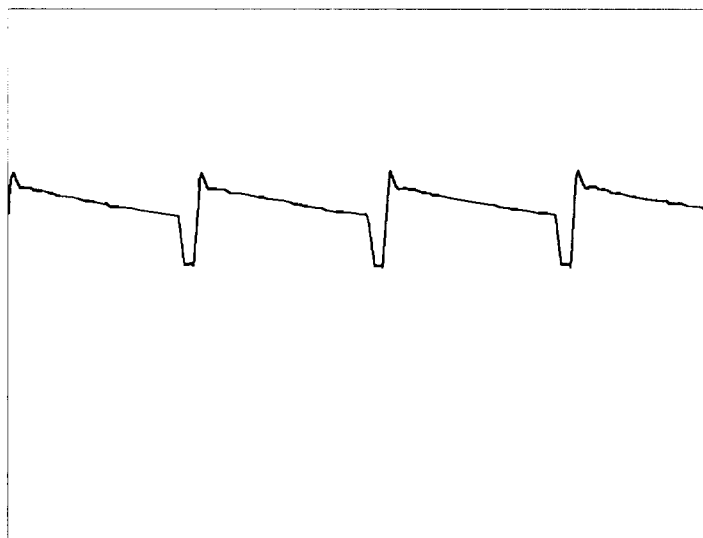
- **The A6 power supply and A6A1 high voltage assemblies contain lethal voltages with lethal currents in all areas. Use extreme care when servicing these assemblies. Always disconnect the power cord from the instrument before servicing these assemblies. Failure to follow this precaution can present a shock hazard which may result in personal injury.**
- **The voltage potential at A6A1W3 is +9 kV. If the cable must be disconnected, always disconnect it at the CRT with caution! Failure to properly discharge A6A1W3 may result in severe electrical shock to personnel and damage to the instrument. See Chapter 3, Procedure 2.**
- **Always use an isolation transformer when troubleshooting either the A6 power supply or the A6A1 HV module. When using an isolation transformer, connect a jumper between A6TP101 and A6TP301. This connects the circuit common to earth ground. Remove this jumper when the isolation transformer is not used.**

---

### Dead Power Supply

1. Use an isolation transformer and connect a jumper between A6TP101 and A6TP301.
2. Connect the negative lead of a DVM to A6TP301.
3. Check TP308 for +5 V.
4. Check TP302 for +15 V.
5. Check TP303 for –15 V.
6. Check TP304 for +28 V.
7. Check TP305 for –12.6 V.
8. Measure the voltage at TP108 to verify the output of the input rectifier. The voltage should be between +215 Vdc and +350 Vdc.
9. If it is not within this range, check the rear panel fuse, input rectifier, input filter, and the rear-panel line voltage selector switch.
10. Measure the voltage at TP206 to verify the output of the kick- start/bias-circuitry. The voltage should be approximately +14 Vdc. Test point 206 is on pin 1 of U203.

11. If there is no voltage at TP206, check TP210 for pulses 200 ms wide with an amplitude of 14.7 V. If there are no pulses present, the kick-start circuitry is probably defective. If the pulses are low in amplitude (about 1 V), Q201 is probably shorted.
12. If there are pulses at TP206, or there are pulses at TP210, but not at TP206, the buck regulator control circuitry is probably faulty.
13. Disconnect the power cord from the HP 8560E spectrum analyzer.
14. Connect the positive output of a current-limited dc power supply to the cathode of A6CR201 (TP206) and the ground to A6TP201.
15. Set the current limit of the power supply to about 500 mA and the voltage to 12 Vdc.
16. Make sure a jumper is connected from A6TP101 to A6TP301. This independently powers the buck regulator control circuitry.
17. Connect a jumper from the dc power supply's +12 Vdc output to the end of A6R202 physically nearest A6C211.
18. Connect a jumper from +12 Vdc to the end of C207 nearest C209.
19. If the current draw exceeds approximately 50 mA, suspect a short in the buck regulator control circuitry or a shorted CR201.
20. Check TP204 for an 80 kHz sawtooth (4 Vp-p).
21. Check TP203 and TP207 for 40 kHz square (12 Vp-p). If the waveforms at either TP203 or TP207 are bad, one of the FETs in the DC-DC Converter is probably defective.
22. Check TP105 and TP106 for a 12 Vp-p sawtooth waveform that is flattened at the bottom. If the waveform is a squarewave, the FET to which the test point is connected has failed or shorted.
23. Check TP202 for 80 kHz pulses (12 Vp-p).
24. Short TP401 to TP102. Check TP103 for a waveform similar to that in Figure 12-4.
25. If the waveform at TP202 is correct but the waveform at TP103 is bad, suspect either Q102 or CR106.



5x1123

**Figure 12-4. Buck Regulator Waveform**

### Line Fuse Blowing

1. If the line fuse blows with the **LINE** switch in the off position, suspect either the input filter or the power switch cable assembly.
2. If the line fuse blows when the HP 8560E spectrum analyzer is turned on, disconnect the power cord and lift the drain of A6Q102 from TP108. If the line fuse still blows, suspect CR102 through CR105.
3. If the fuse is not burned out, check A6TP108 for a voltage of between +215 V and +350 V.
4. If the voltage at TP108 is correct, disconnect the power cord. Wait 60 seconds for the high voltage to discharge. Remove and check A6Q102.
5. If Q102 is shorted, Q103, Q104, CR106, and CR108 are also probably shorted. If Q102 is working properly, measure the resistance between TP102 and TP101 (positive ohmmeter lead to TP102).
6. If the resistance is less than 1 k $\Omega$ , suspect either Q103 or Q104 in the DC-DC Converter.

### Supply Restarting Every 1.5 Seconds (Kick Start)

See function blocks G, H and L of A6 power supply schematic diagram in the component-level information binder.

If there is a short on the power supply or on one of the other assemblies, the power supply will attempt to “kick start.” (Every 1.5 seconds the supply will attempt to start, but will be shut down by a fault condition.) The kick start and bias circuits provide power for the control circuitry during power-up. The kick start circuitry is an RC oscillator which emits a 200 ms pulse every 1.5 seconds. These pulses switch current from the Input Rectifier through Q201 to charge C201. When the power supply is up, a winding on T103 provides power to the control circuitry. This voltage is high enough to keep Q201 turned off.

1. Monitor the waveforms at TP206 and TP208 simultaneously on an oscilloscope.
2. If the signal at TP208 goes high before the signal at TP206 goes low, an overcurrent condition has been detected. Suspect a short in the secondary (output rectifier, voltage regulators, or another assembly).

### Low Voltage Supplies

1. Connect the DVM's negative lead to A6TP301.
2. Check A6TP302 for +15 Vdc.
3. Check A6TP303 for -15 Vdc.
4. Check A6TP304 for +28 Vdc.
5. Check A6TP305 for -12.6 Vdc.
6. Check A6TP308 for +5 Vdc.
7. If the voltages measured above are correct but the power supply LEDs on the A2 controller assembly are not lit, check W1.
8. If the voltages are low, disconnect W1 from A6J1 and measure the test point voltages again. Unless a dummy load is connected to the A6 power supply, the voltages should return to their nominal voltages but be unregulated.
9. If the voltages do not return to near their nominal range, the A6 power supply is probably at fault.
10. If the +5 V supply is low, suspect the +5 V regulator or the feedback circuit. To check the feedback circuit, measure the voltage of the +5 V reference (U305 pin 6) and the  $\pm 5$  V references to the voltage regulators (U306B pin 7 and U306D pin 14).
11. Check output of U306A pin 1. If the feedback circuit is working properly, the output of U306A should be near +13 Vdc.
12. Check output of U302; its output should be high if the feedback circuit is working properly.

### High Voltage Supplies

1. Press **LINE** to turn spectrum analyzer off, disconnect the power cord, and remove the power supply shield.
2. Connect a DVM's negative lead to A6TP401 and positive lead to A6TP405.
3. Press **LINE** to turn spectrum analyzer on.
4. If the voltage displayed on the DVM is approximately +110 Vdc and the rear-panel CRT +110 VDC ON indicator is lit, the A6A1 HV module is probably at fault.

---

#### Note

Ideally, the DVM should read the voltage written on the label of the A6A1 HV module. If necessary, perform the "High Voltage Power Supply" adjustment in Chapter 2.

---

5. If the DVM does not read approximately +110 Vdc, measure the voltage on A6U401 pin 10. This is the HV\_SHUT\_DOWN signal and should be near +5 Vdc.
6. If HV\_SHUT\_DOWN is low, suspect a bad connection along W8 between the A6 power supply and the 17 CRT driver.
7. If HV\_SHUT\_DOWN is correct, connect an oscilloscope to A6TP402. Connect the scope probe's negative lead to TP401. Set the oscilloscope to the following settings:
 

|                      |                |
|----------------------|----------------|
| Sweep time .....     | 10 $\mu$ s/div |
| Vertical scale ..... | 10 V/div       |
8. A nearly-sinusoidal waveform, greater than 30 Vp-p, with an approximately +18 Vdc offset, should be observed.
9. If the waveform is a dc voltage near 0 Vdc with narrow, positive- and negative-going pulses, the A6A1 HV module is faulty. If the waveform is a dc voltage near +18 Vdc with narrow, positive- and negative-going pulses, connect the probe to TP403.
10. If the waveform at TP403 is a sawtooth waveform with a 1.8 V amplitude, the A6A1 HV module is faulty.
11. If the TP403 waveform has pulses similar to those on TP402, the A6 power supply is probably faulty.

### CRT Supply Dropping Out

See function block K of A6 power supply schematic diagram in the component-level information binder.

The CRT supply is a separate switching supply which provides the +110 Vdc for the A17 CRT driver from a winding on the A6A1 HV module. The CRT supply operates at approximately 30 kHz. The exact frequency is determined by the inductance of the primary winding of A6A1T1 and A6C407. The supply will only operate if the HV\_SHUT\_DOWN line is high.

If the power supply keeps dropping out, there is probably a short on the A17 CRT driver assembly.

1. Disconnect W8 from A6J4.
2. Connect an IC clip to U401 and connect a jumper between U401 pin 10 and TP308 (+5 Vdc).
3. Connect a voltmeter to TP405 and press **LINE** to turn the spectrum analyzer on.
4. Check TP405 for a voltage of approximately +110 Vdc. It will probably measure higher since there is no load on the supply.
5. If the voltage at TP405 is correct, suspect a short on A17. If the voltage at TP405 is not correct, check U401 pin 8 for a sawtooth signal. The sawtooth should be flat-topped and about 5 Vp-p at a frequency of about 30 kHz.
6. If the sawtooth is not flat-topped, suspect U402A and its associated circuitry.
7. If the sawtooth is correct, check the base of Q401 for 30 kHz pulses.
8. If the duty cycle is high, but there is no +110 Vdc, suspect the bridge rectifier, CR401 through CR404.

## Blanking Signal

1. Connect an oscilloscope probe to A2J202 pin 3. Connect the oscilloscope ground lead to TP3. Set the oscilloscope to the following settings:  
Sweep time ..... 2 ms/div  
Vertical scale ..... 1 V/div
2. If a 4 Vp-p signal is not observed, the A2 controller assembly is faulty.
3. Repeat steps 1 and 2 with the oscilloscope probe on A2J202 pin 14.
4. Set the oscilloscope to the following settings:  
Sweep time ..... 1  $\mu$ s/div  
Vertical scale ..... 2 V/div
5. Connect the positive probe lead to A2J202 pin 15. This is the blanking output.
6. TTL-level pulses should be observed. If the signal is either always high or always low, the display will be blanked; suspect the A2 controller assembly.
7. If the signals on A2J202 pins 3, 14, and 15 are correct, troubleshoot the A17 CRT driver.

## Buck Regulator Control

See function block H of the A6 power supply schematic diagram in the component-level information binder.

The buck regulator control pulse-width modulates the buck regulator and provides a synchronized signal to the DC-DC converter control circuitry. The buck regulator control has two feedback paths. The first is the output of the buck regulator, which provides coarse regulation. The second is the feedback circuit which samples and compares the +5 Vdc output of the output rectifier.

U202B and associated circuitry sense the output of the input rectifier and will turn off U203 if the voltage at TP108 goes below approximately +170 Vdc. Also, it will not allow U203 to start up until this voltage exceeds +215 Vdc. A low on the output of U202B will also clear the overcurrent latch in the DC-DC converter control circuitry.

Thermal shutdown occurs when RT201, mounted on the main heatsink, reaches a temperature of 100 C. When this occurs, the voltage at U203 pin 13 exceeds 0.6 V and inhibits pulses to the buck regulator.

R203, R204, U211, and associated circuitry provide feedforward for U203. This makes the loop gain independent of input line voltage and cancels 120 Hz ripple by more than 10 dB.

U202C and its associated circuitry permit the power supply to start up at low line voltages at low temperatures. At low line voltages U202C will draw charge away from C206 through R205. This allows the buck regulator to turn on and draw current through the thermistors in the input rectifier. This warms up the thermistors, thereby decreasing their resistance and increasing the voltage at TP108. When the voltage is sufficiently high at TP108, the output of U202C will open and C206 will be allowed to charge normally.

U202A converts the sawtooth at TP204 to a squarewave to drive the DC-DC Converter Control circuitry. The frequency of the sawtooth is determined by the resistance at pin 7 of U203 and the capacitance at pin 8 of U203.

## **DC-DC Converter Control**

See function block I of A6 power supply schematic diagram in the component-level information binder.

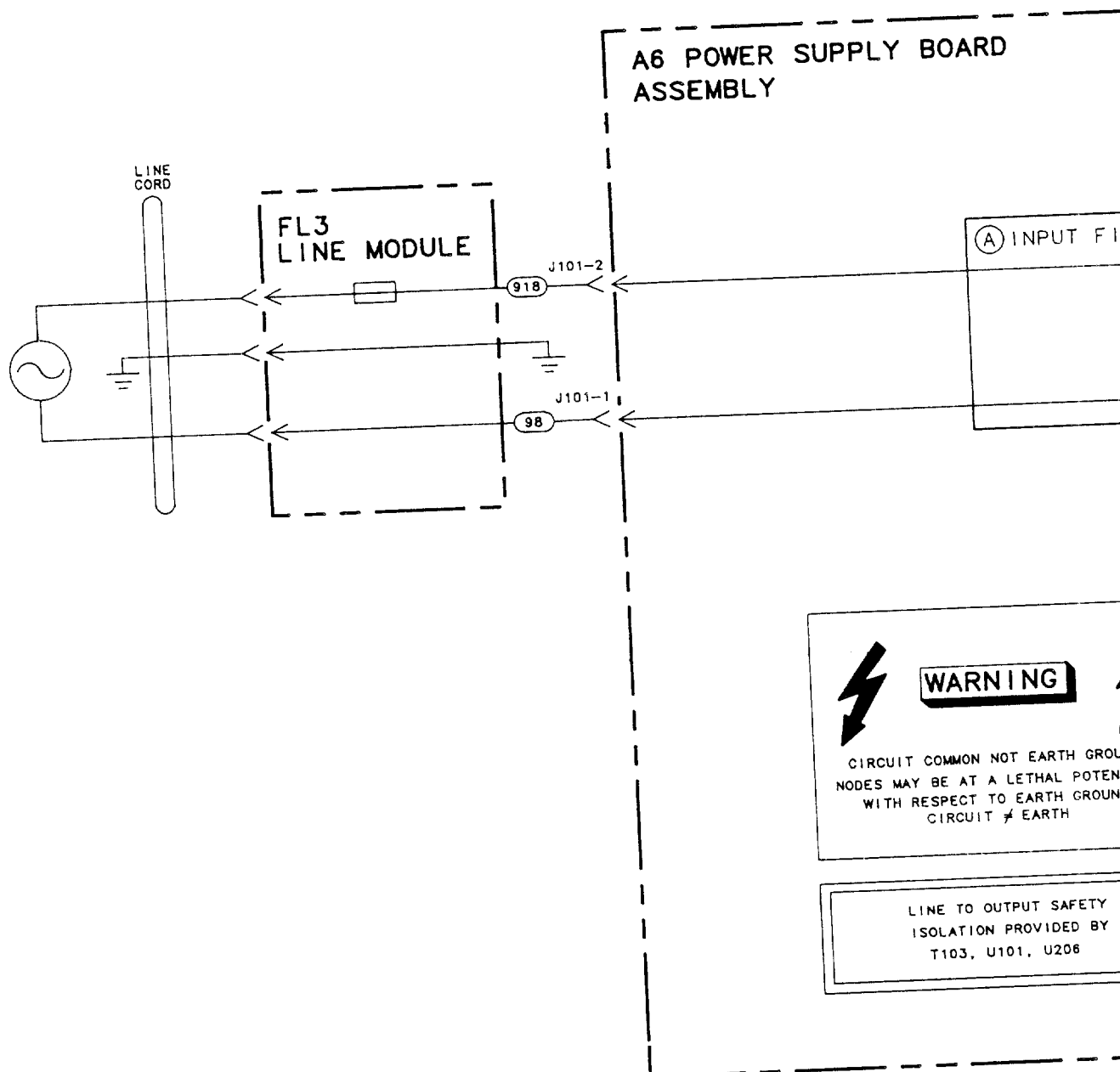
The DC-DC converter control circuitry divides the 80 kHz squarewave from U202A and generates two complementary 40 kHz squarewaves to drive the FETs in the DC-DC converter. Also, U202D and its associated circuitry monitor the voltage across sense resistor R116 in the DC-DC converter. When the current through the FETs in the DC-DC converter exceeds 1.8 A, the voltage across R116 will cause the output of U202D to go high. This sets a latch in U204 which turns off U203.

## **Power Up**

See function block M of the A6 power supply schematic diagram in the component-level information binder.

The power up circuitry generates the PWR UP signal, which tells the microprocessor that the supplies are up and stable. PWR UP will go high when the +5 Vdc supply exceeds +4.99 Vdc. PWR UP will go low when this voltage drops below +4.895 Vdc. Once PWR UP is set low, it will stay low for at least 50 ms before going high, even if the +5 Vdc supply exceeds +4.99 Vdc before 50 ms have elapsed.

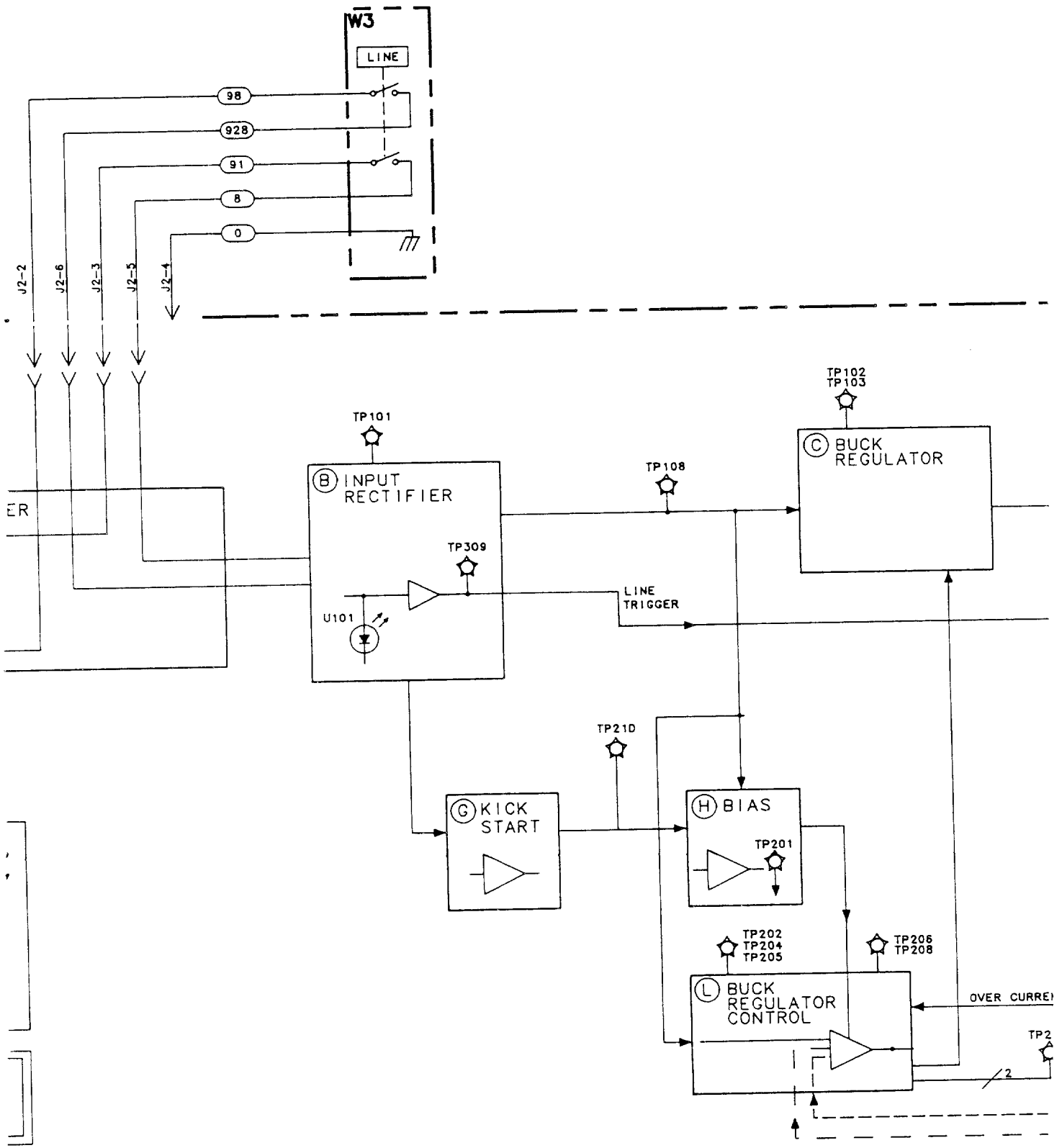
# POWER SUPPLY ASSEMBLY BLOCK DIAGRAM

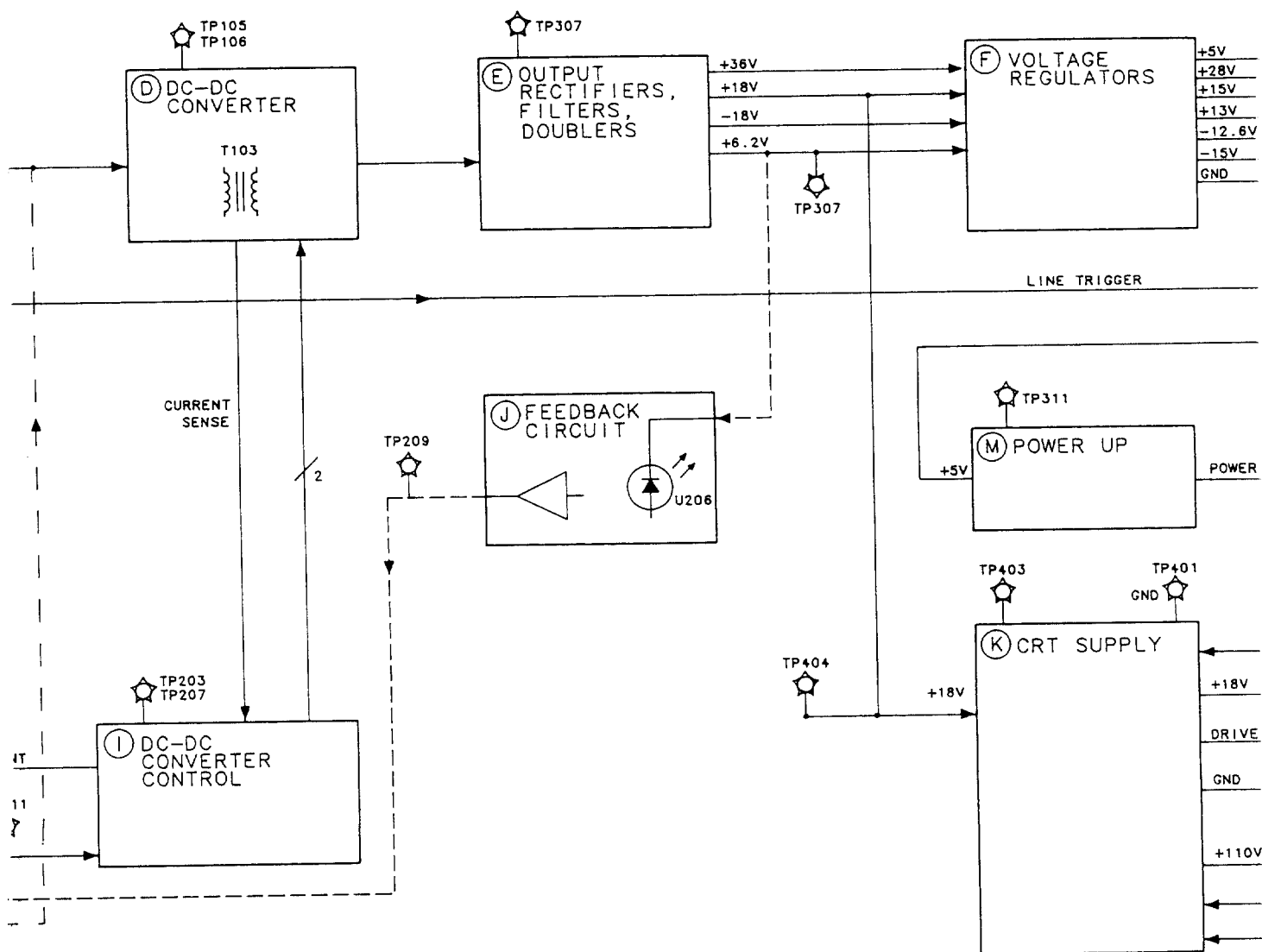


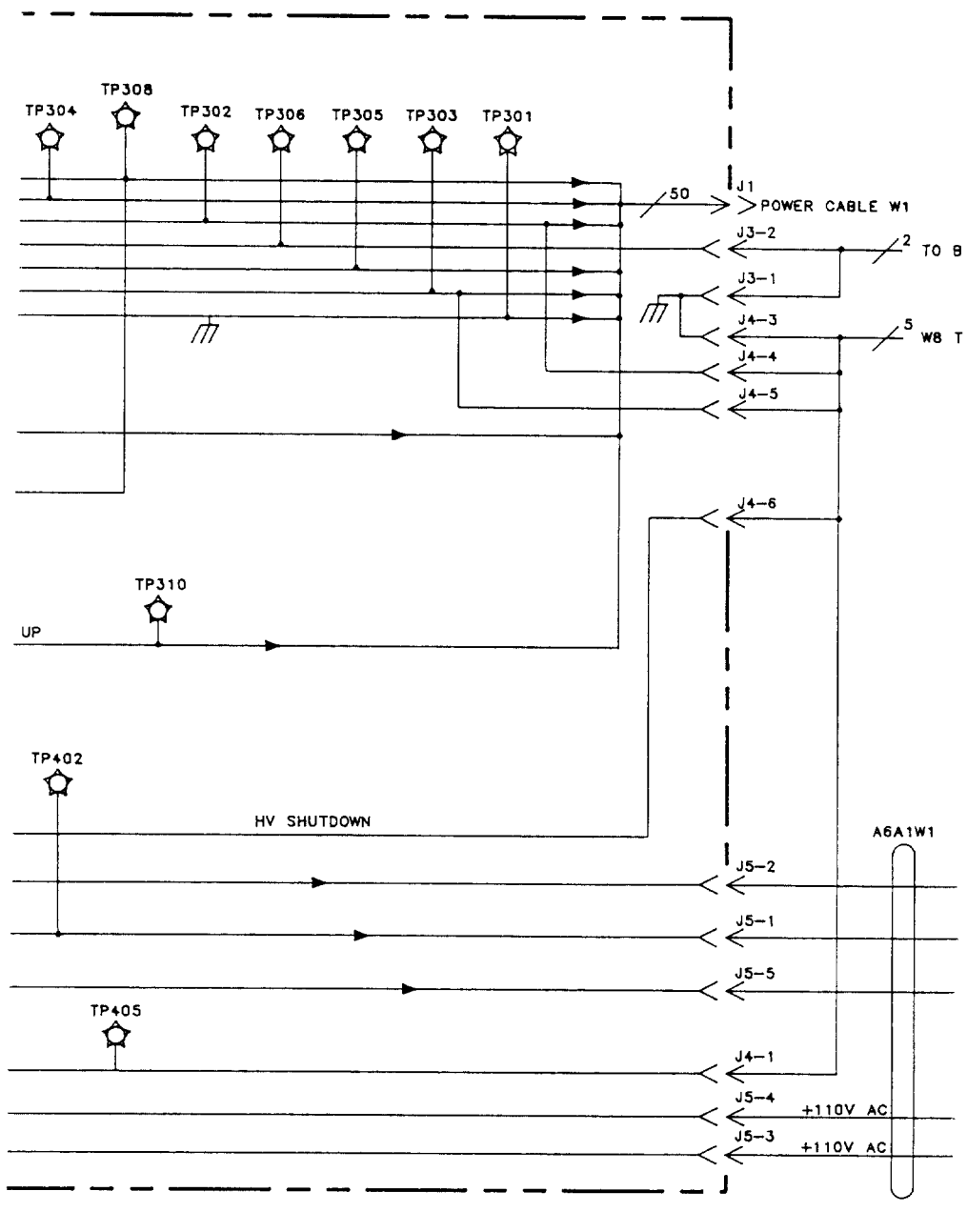
## WARNING

CIRCUIT COMMON NOT EARTH GROUND  
NODES MAY BE AT A LETHAL POTENTIAL  
WITH RESPECT TO EARTH GROUND  
CIRCUIT ≠ EARTH

LINE TO OUTPUT SAFETY  
ISOLATION PROVIDED BY  
T103, U101, U208







1 (FAN)

O A17 CRT DRIVER

**WARNING**

HAZARDOUS  
VOLTAGE

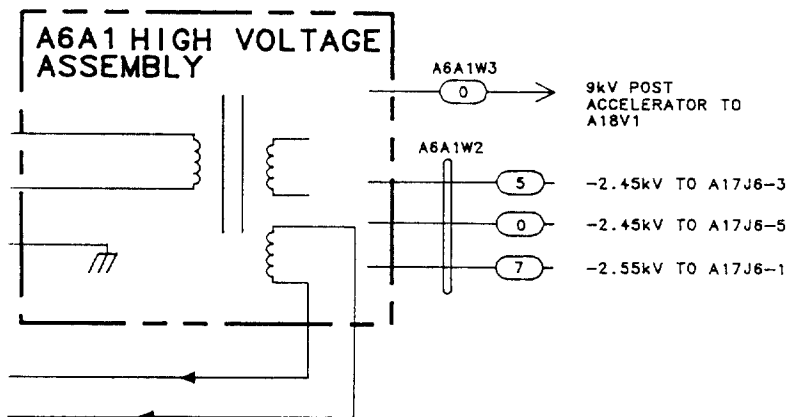
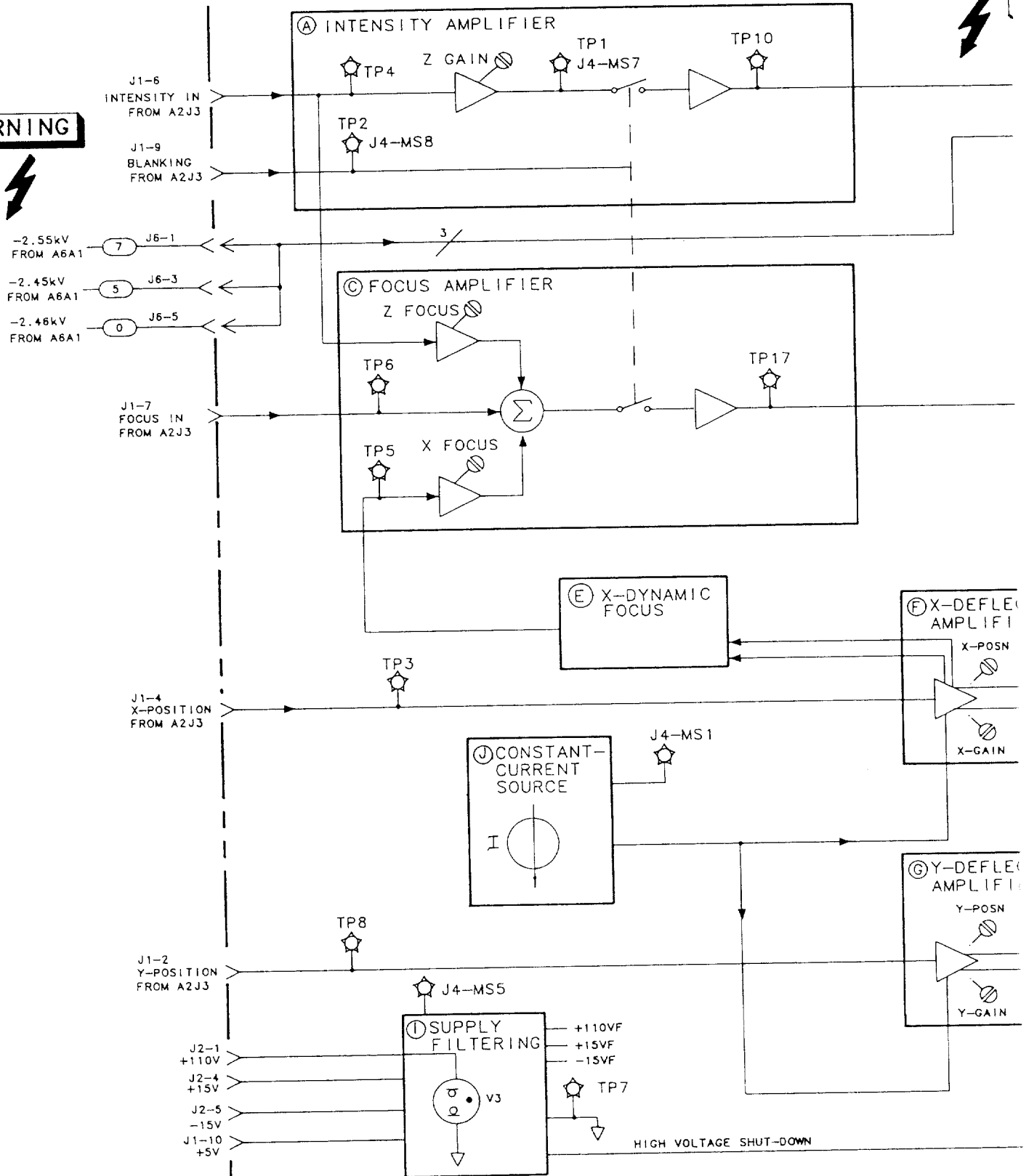


FIGURE 12-5. A6 POWER SUPPLY BLOCK DIAGRAM

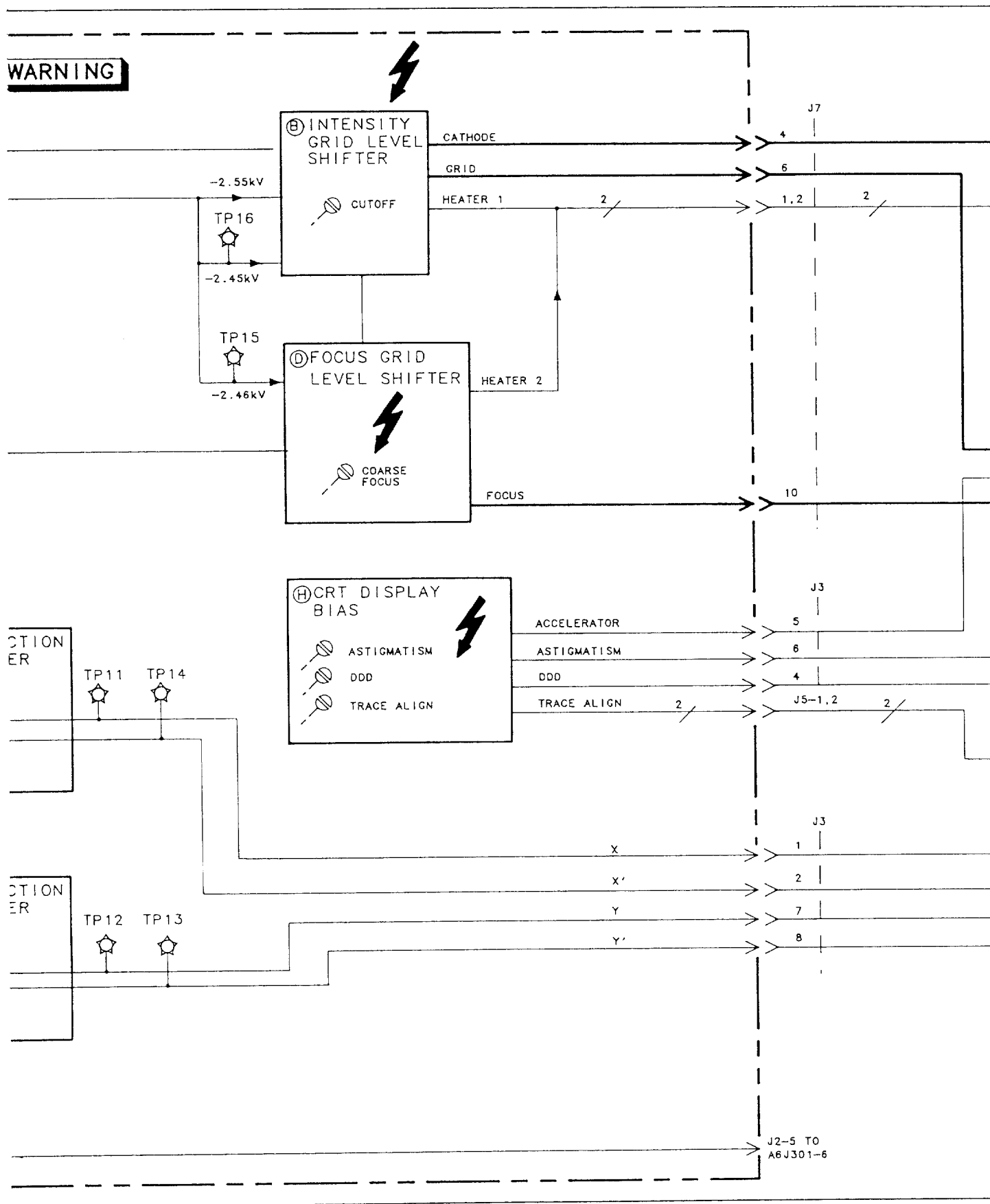
# A17 CRT DISPLAY DRIVER BLOCK DIAGRAM

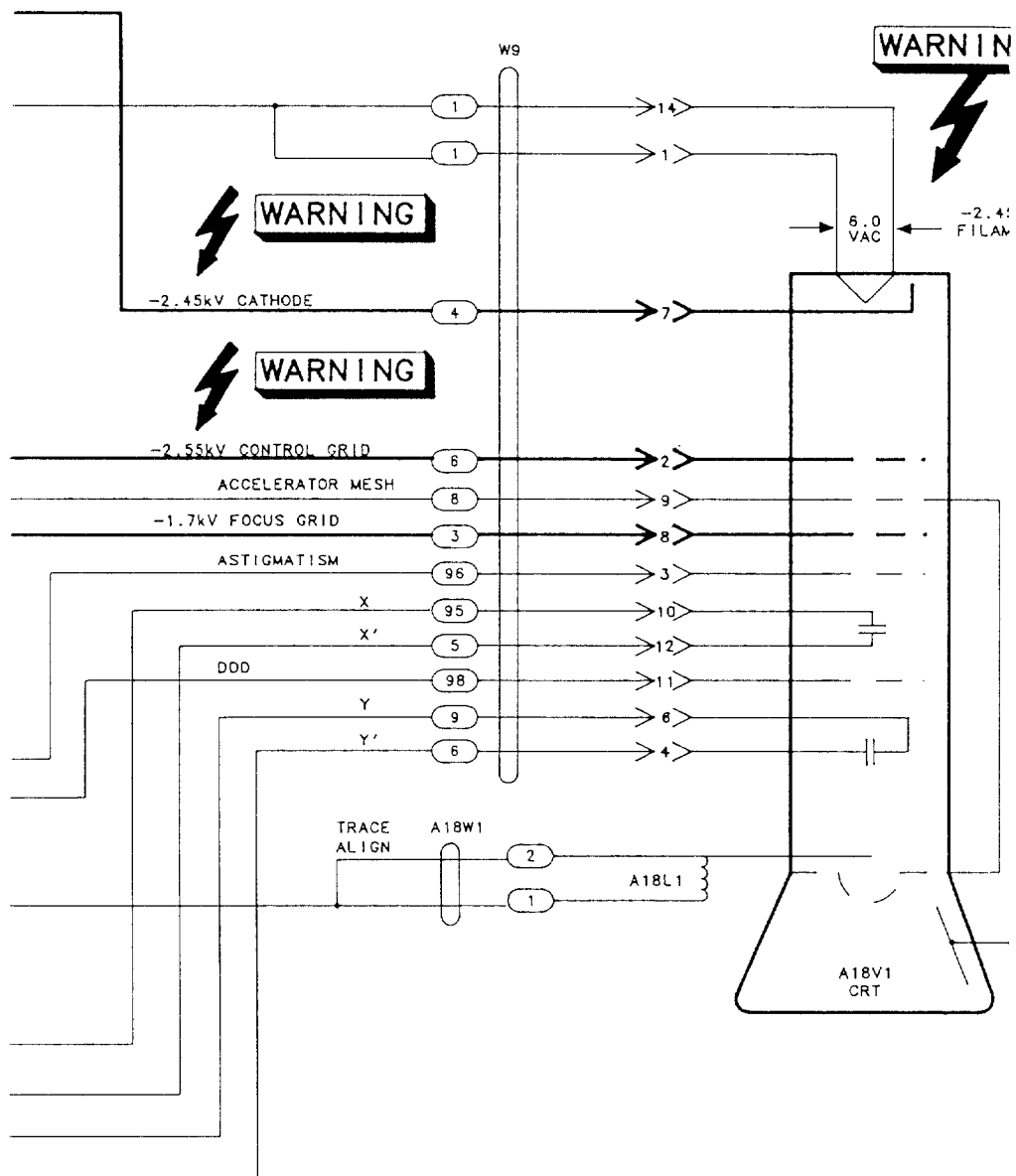
# A17 CRT DISPLAY DRIVER

**WARNING**



**WARNING**

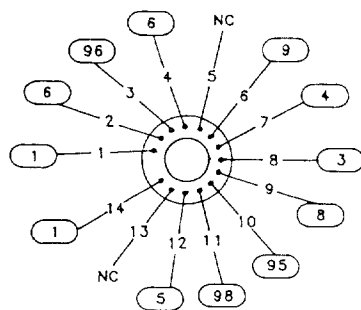




**WARNING HIGH VOLTAGE**  
 DISCONNECT AT CRT WITH CAUTION!  
 DISCHARGE FIRST BY GROUNDING AT  
 CRT CONNECTION!

**G**

3kV  
IDENT



**CRT CONNECTOR  
(REAR VIEW)**

**WARNING**



←5 0 A6A1W3  
POST +9kV  
ACCELERATOR FROM A6A1



FIGURE 12-6. A17 CRT DRIVER BLOCK DIAGRAM

## Component-Level Information Packets

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Component-Level information is available for selected instrument assemblies. The information for each repairable assembly is provided in the form of Component-Level Information Packets (CLIPs). Each CLIP contains a parts list, component-location diagram, and schematic diagram. Each CLIP has an HP part number which is changed whenever the HP part number for its related instrument assembly is changed.

Updated or replacement CLIPs may be ordered through your local Hewlett-Packard Sales or Service office using the CLIP part number provided in Table A-1.

A complete set of the latest version of CLIPs can be ordered using HP part number 5960-6550.

---

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <b>Note</b> | CLIPs may not be available for recently introduced assemblies. |
|-------------|----------------------------------------------------------------|

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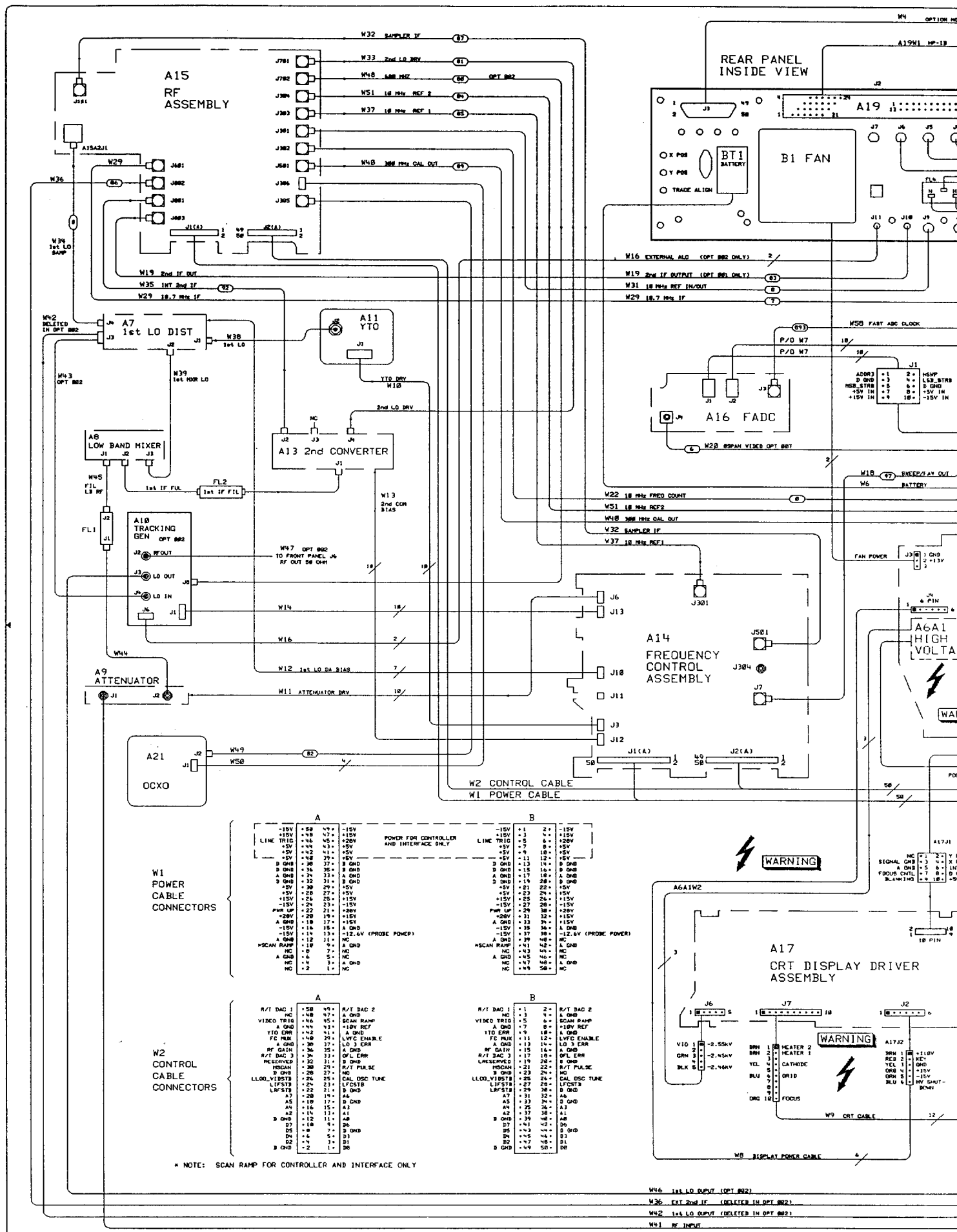
**Table A-1. HP 8560E Spectrum Analyzer Documented Assemblies**

| Board Assembly                                                                                                                                                                                                                                                                                    | Instrument Serial Prefix                                      | Assembly Part Number                                   | CLIP Part Number                                  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|--------------------------------------------------------|---------------------------------------------------|
| A1A1 Keyboard                                                                                                                                                                                                                                                                                     | 3213A and above                                               | 08562-60140                                            | <b>08562-90188*</b>                               |
| A2 Controller Assembly                                                                                                                                                                                                                                                                            | 3213A through 3305A<br>3310A and above                        | 08563-60017<br>08563-60032 <sup>†</sup>                | 08563-90055<br><b>08563-90074*</b>                |
| A3 Interface Assembly<br>(non-Option 007)                                                                                                                                                                                                                                                         | 3213A and above                                               | 08563-60021                                            | <b>08563-90056*</b>                               |
| A3 Interface Assembly<br>(Option 007)                                                                                                                                                                                                                                                             | 3310A and above                                               | 08563-60033                                            | <b>08563-90075*</b>                               |
| A4 Log Amplifier/Cal Osc                                                                                                                                                                                                                                                                          | 3213A through 3246A<br>3301A and above                        | 08563-60025<br>08563-60050 <sup>†</sup>                | 08563-90057<br><b>08563-90082*</b>                |
| A5 IF Filter                                                                                                                                                                                                                                                                                      | 3213A and above                                               | 08563-60023                                            | <b>08563-90058*</b>                               |
| A6 Power Supply                                                                                                                                                                                                                                                                                   | 3213A and above                                               | 08563-60020 <sup>†</sup>                               | <b>08562-90059*</b>                               |
| A14 Frequency Control                                                                                                                                                                                                                                                                             | 3213A through 3305A<br>3310A and above                        | 08560-60059<br>08560-60062 <sup>†</sup>                | 08560-90082<br><b>08560-90084*</b>                |
| A15 RF Board (Option 103)<br>(With SIG ID);                                                                                                                                                                                                                                                       | 3213A through 3221A<br>3240A through 3304A<br>3305A and above | 08563-60010<br>08563-60035<br>08563-60045 <sup>†</sup> | 08563-90062<br>08563-90068<br><b>08563-90072*</b> |
| <p>*Denotes the current version of board assembly.<br/> <sup>†</sup>Denotes refurbished board assemblies available. Refurbished board assembly part numbers have 9 as the second digit of the suffix. For example, 08563-69032 is the refurbished part number for board assembly 08563-60032.</p> |                                                               |                                                        |                                                   |

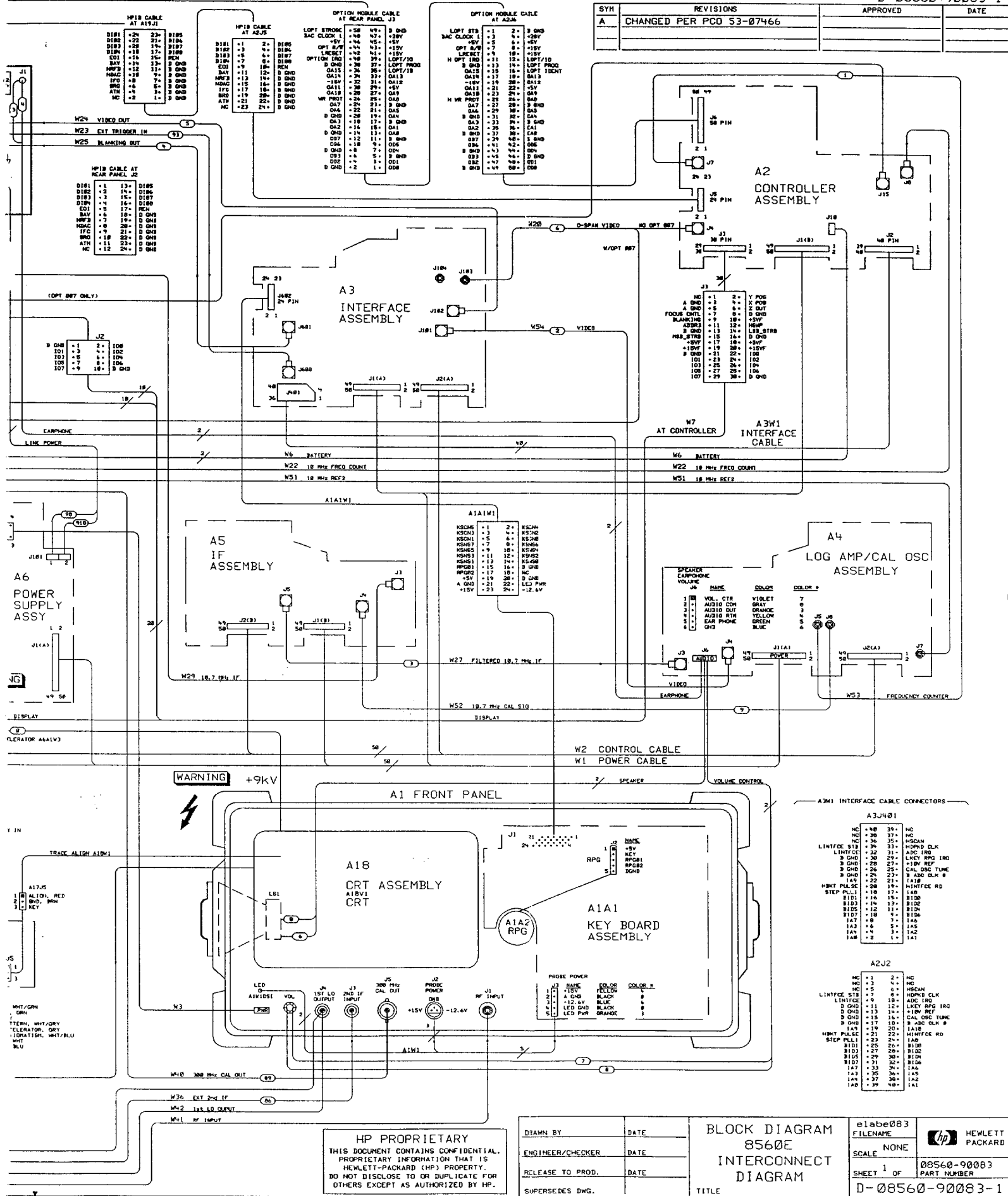
**Table A-1.**  
**HP 8560E Spectrum Analyzer Documented Assemblies (continued)**

| Board Assembly                                                                                                                                                                                                                                                                                      | Instrument<br>Serial Prefix                                   | Assembly<br>Part Number                                | CLIP Part Number                                  |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|--------------------------------------------------------|---------------------------------------------------|
| A15 RF Board (Option 103)<br>(Without SIG ID)                                                                                                                                                                                                                                                       | 3305A and above                                               | 08563-60043 <sup>†</sup>                               | <b>08563-90070*</b>                               |
| A15 RF Board (Standard)<br>(With SIG ID)                                                                                                                                                                                                                                                            | 3213A through 3221A<br>3240A through 3304A<br>3305A and above | 08563-60016<br>08563-60036<br>08563-60046 <sup>†</sup> | 08563-90061<br>08563-90069<br><b>08563-90073*</b> |
| A15 RF Board (Standard)<br>(Without SIG ID)                                                                                                                                                                                                                                                         | 3305A and above                                               | 08563-60044 <sup>†</sup>                               | <b>08563-90071*</b>                               |
| A16 Fast ADC                                                                                                                                                                                                                                                                                        | 3310A and above                                               | 08563-60030                                            | <b>08563-90076*</b>                               |
| A17 CRT Driver                                                                                                                                                                                                                                                                                      | 3213A<br>3221A and above                                      | 08562-60165<br>08562-60166                             | 08562-90187<br><b>08562-90193*</b>                |
| A19 HP-IB                                                                                                                                                                                                                                                                                           | 3213A and above                                               | 08562-60042                                            | <b>08562-90115*</b>                               |
| <p>* Denotes the current version of board assembly.<br/> <sup>†</sup> Denotes refurbished board assemblies available. Refurbished board assembly part numbers have 9 as the second digit of the suffix. For example, 08563-69032 is the refurbished part number for board assembly 08563-60032.</p> |                                                               |                                                        |                                                   |





| SYN | REVISIONS                | APPROVED | DATE |
|-----|--------------------------|----------|------|
| A   | CHANGED PER PCO 53-07466 |          |      |



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|------------------|------|
| DESIGNED BY      | DATE |
| ENGINEER/CHECKER | DATE |
| RELEASE TO PROD. | DATE |
| SUPERSEDES DWG.  |      |

BLOCK DIAGRAM  
8560E  
INTERCONNECT  
DIAGRAM

|             |                 |    |                    |
|-------------|-----------------|----|--------------------|
| elabe083    | FILENAME        | HP | HEWLETT<br>PACKARD |
| SCALE       | NONE            |    |                    |
| SHEET 1 OF  | 08560-90083     |    |                    |
| PART NUMBER | D-08560-90083-1 |    |                    |

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